

ZZZ1



LA-6001P

DAZ0CG00100

Compal Confidential

NBLB3/5 Schematics Document

Intel Clarksfield Processor with DDRIII + Ibex HM55

2010-04-28

REV:1.0

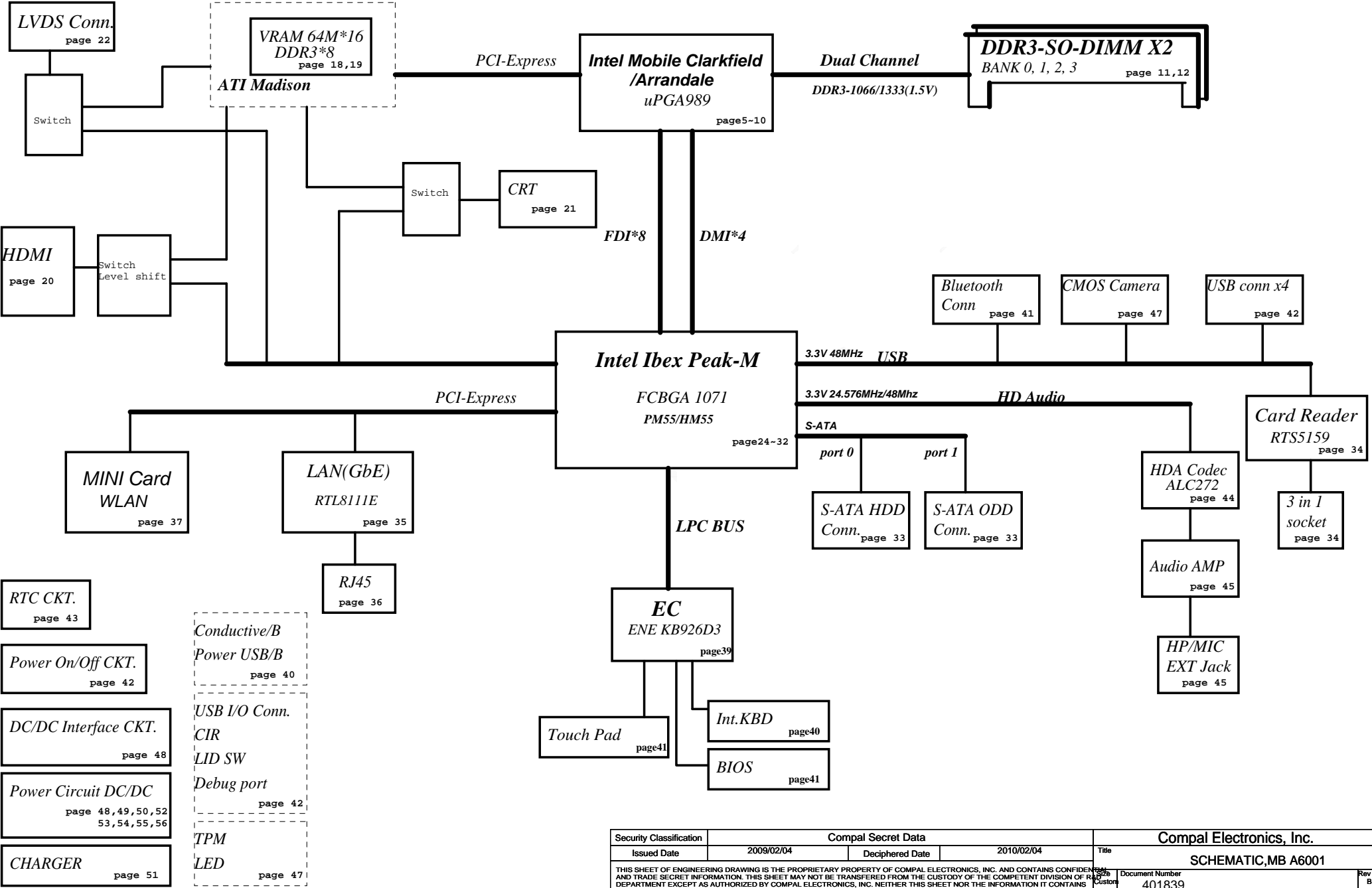
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/02/04	Deciphered Date	2010/02/04	Title	SCHEMATIC,MB A6001	
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				Custom	401839	B
				Date: Thursday, June 10, 2010	Sheet 1 of 59	E

Compal Confidential

Model Name : NBLB3/5

File Name : LA-6001P(Madison)

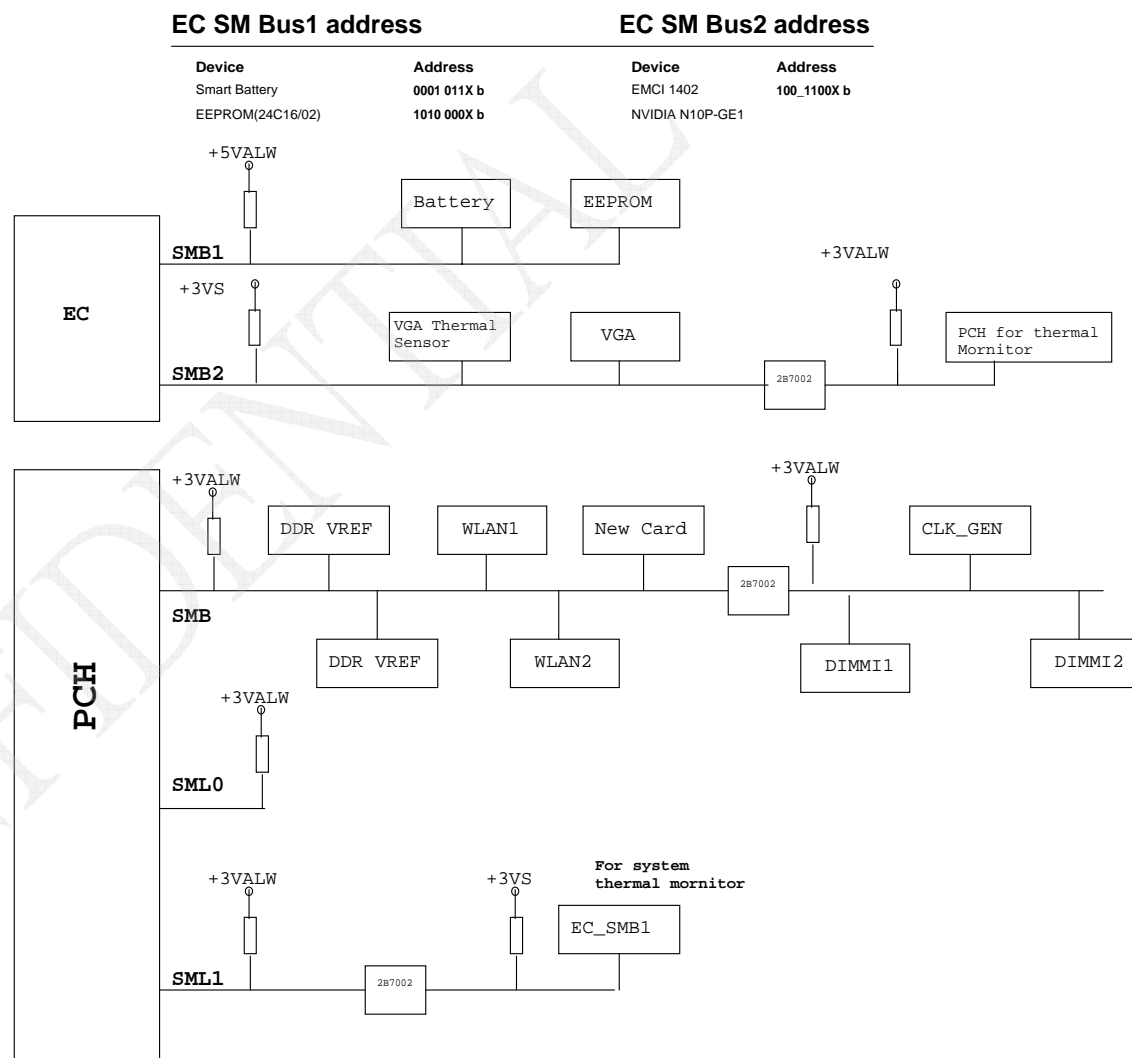
Clock Gen.
SLG8SP587
9LRS3199AKLFT
page23



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power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS +1.1VS_VTT +1.5VS_VRAM
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

	ID3	ID2	ID1	ID0
NBLB2(1100)	R358	R361	R766	R765
Reserve (1101)	X	X	X	X
Reserve (1110)	X	X	X	X
Reserve (1111)	X	X	X	X
NBLB1 (0000)	R353	R350	R766	R765
Reserve(0001)	X	X	X	X
Reserve(0010)	X	X	X	X
Reserve(0011)	X	X	X	X
Reserve(0100)	X	X	X	X
Reserve(0101)	X	X	X	X
Reserve(0110)	X	X	X	X
Reserve(0111)	X	X	X	X
Reserve (1000)	X	X	X	X
Reserve (1001)	X	X	X	X
Reserve (1010)	X	X	X	X
Reserve (1011)	X	X	X	X



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				Document Number	B
				Date: Thursday, June 10, 2010	Sheet 3 of 59

VGA (Madison)

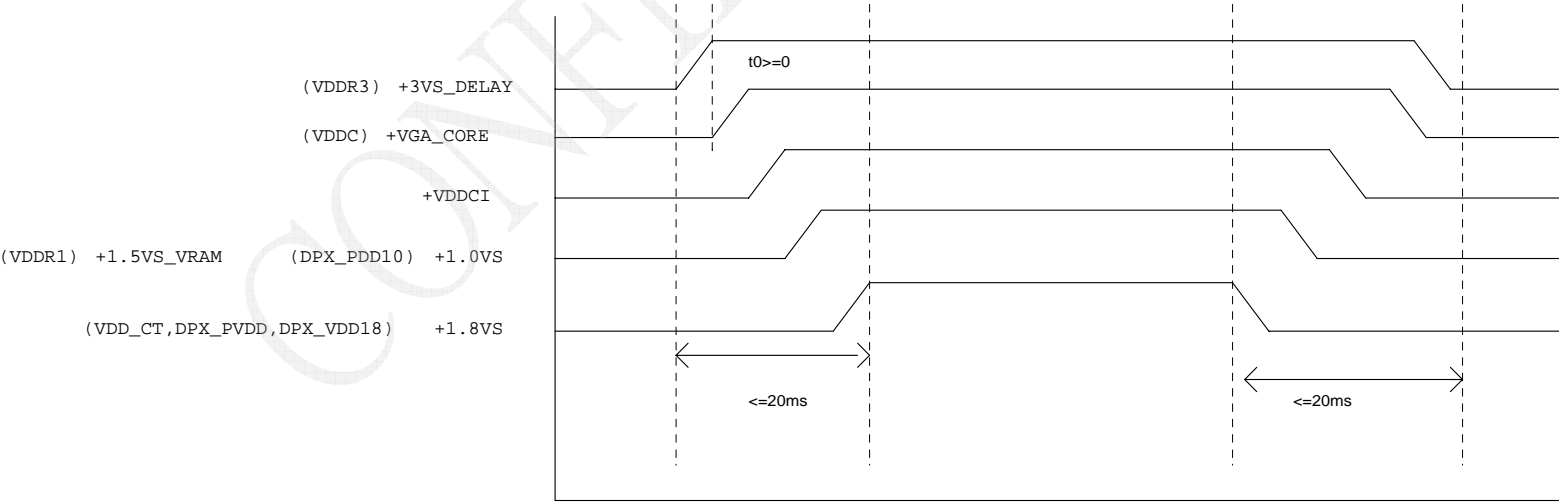
State \ power plane	+1.8VS +1.5VS_VRAM	+3VS_DELAY +VGA_CORE +1.1VS
S0	O	O
S1	O	O
S3	X	X
S5 S4/AC	X	X
S5 S4/ Battery only	X	X
S5 S4/AC & Battery don't exist	X	X

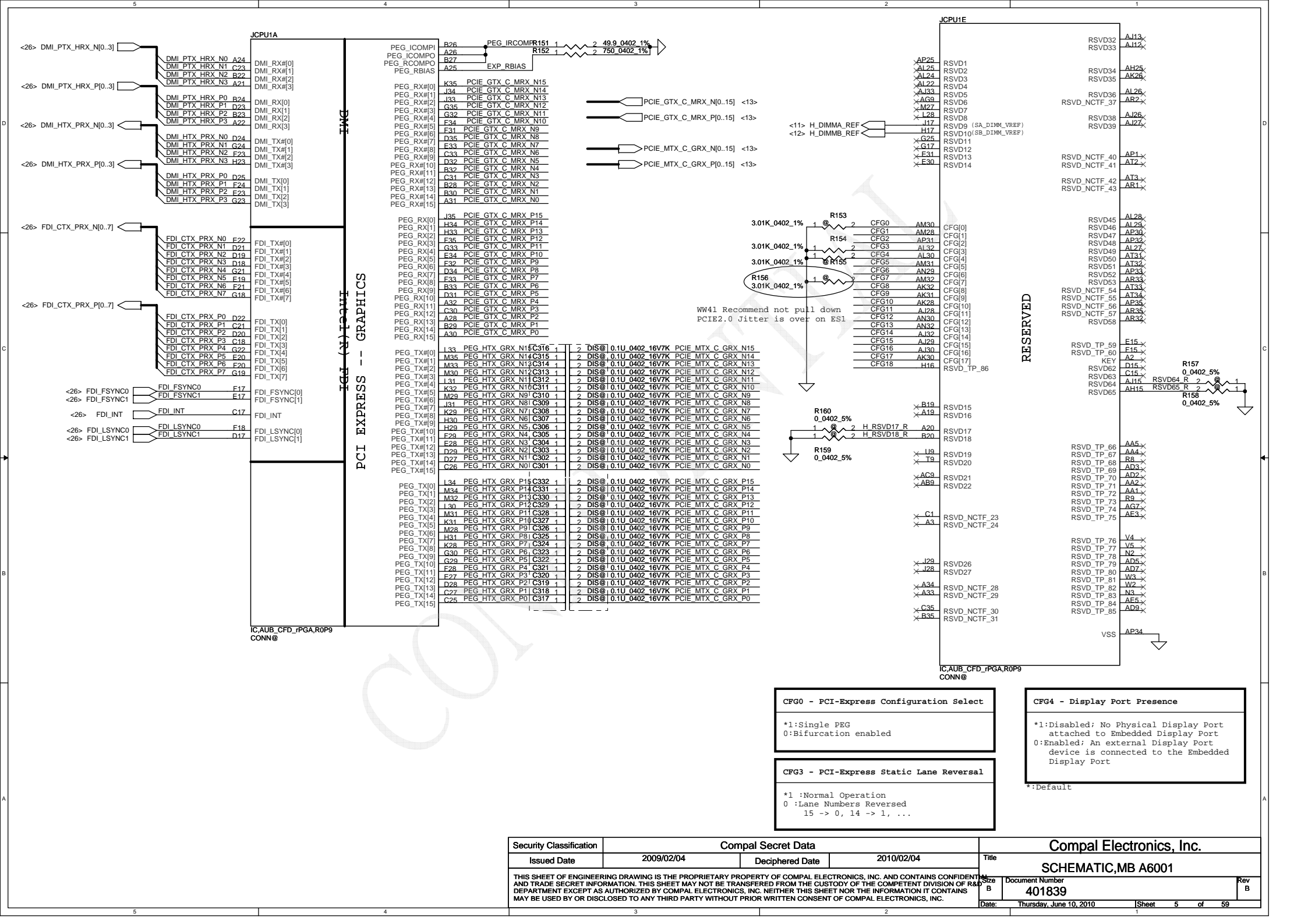
POWER UP/DOWN Sequence

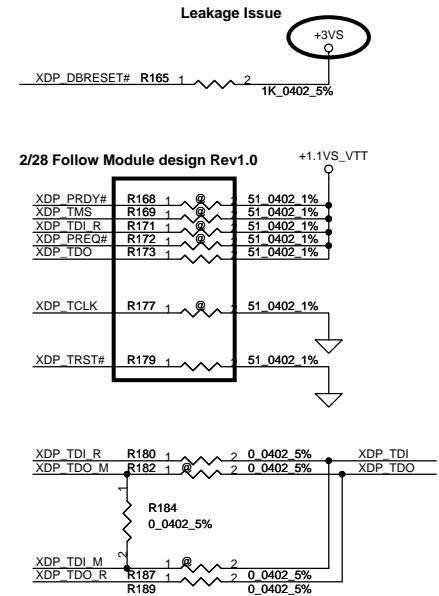
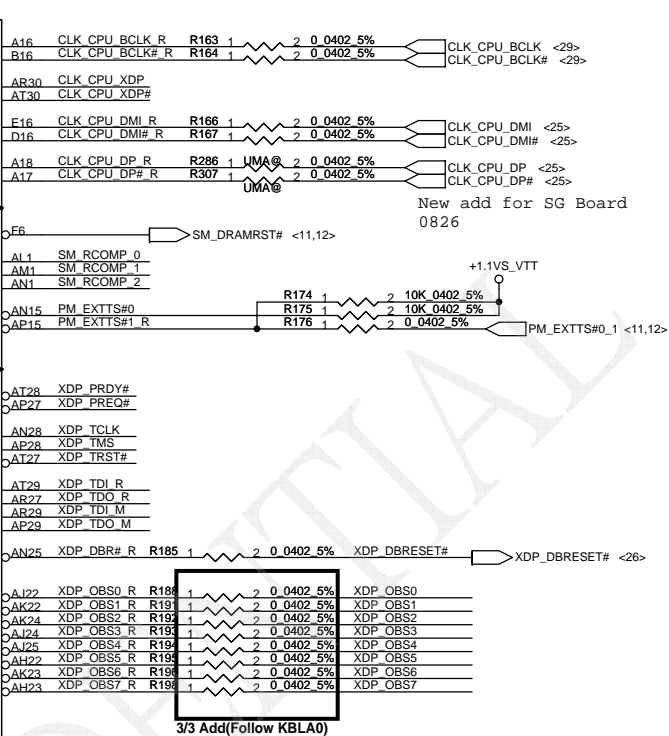
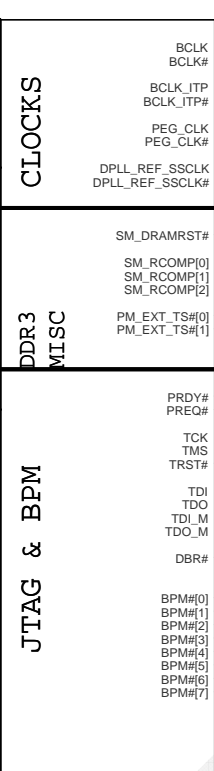
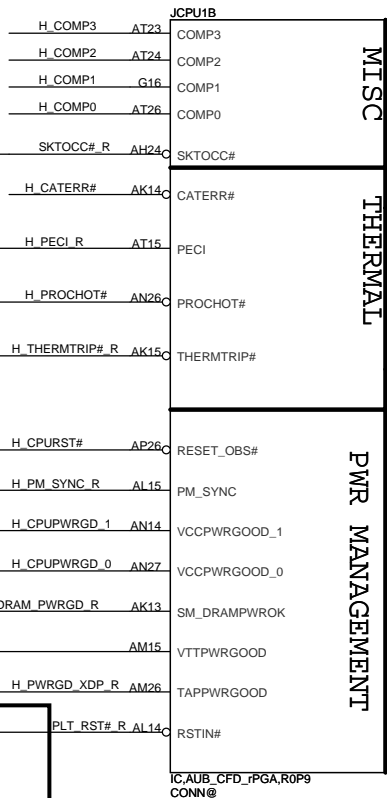
47132_madison_ds_nda_1.04

Madison sequence

- Power-Up/Down Sequence
Madison has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.
- 1, All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
 - 2, VDDR3 should ramp-up before or simultaneously with VDDC.
 - 3, For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
 - 4, The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
 - 5, VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)
 - 6, For power-down, reversing the ramp-up sequence is recommended.



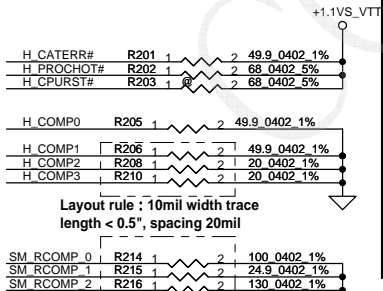
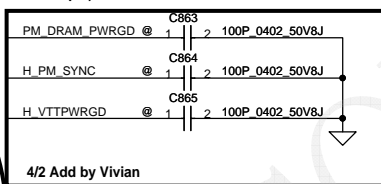
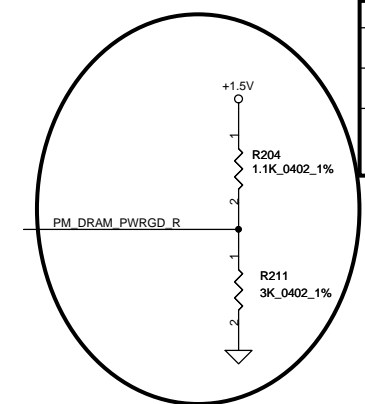




JTAG MAPPING

Scan Chain (Default)	STUFF -> R653, R657, R662 NO STUFF -> R655, R660
CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
GMCH Only	STUFF -> R660, R662 NO STUFF -> R653, R655, R657

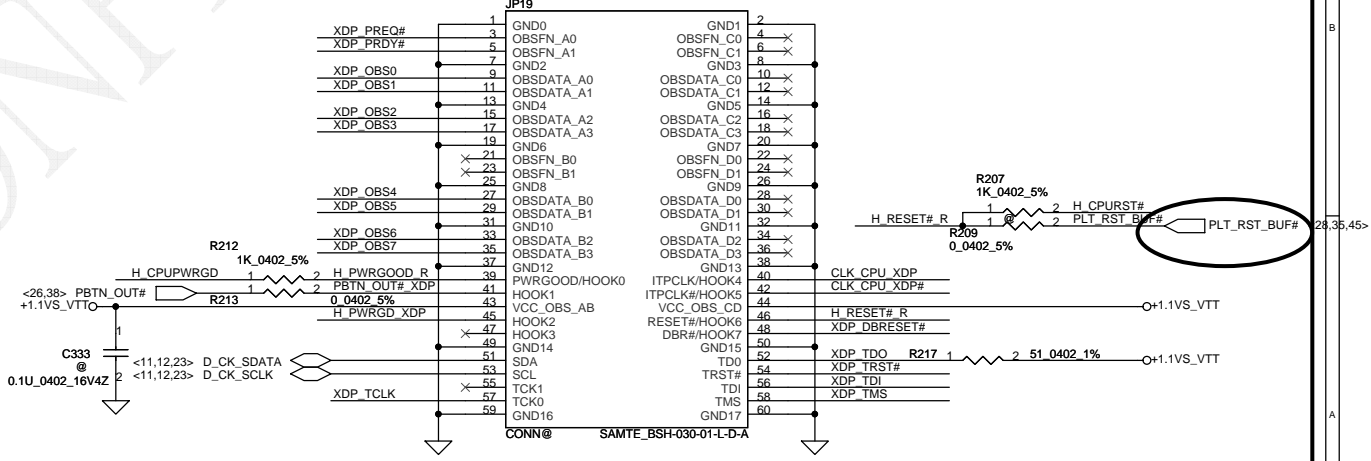
4/17 Modify R199 to 1.5K ohm, R200 to 750 ohm(see DG414044 p.8)



DDR3 Compensation Signals

Layout Note: Please these resistors near Processor

XDP Connector



<11> DDR_A_D0[0..63]
<11> DDR_A_DM[0..7]
<11> DDR_A_DQS#0[0..7]
<11> DDR_A_DQS#0[0..7]
<11> DDR_A_MA[0..15]

DDR_A_D0 A10
DDR_A_D1 C10
DDR_A_D2 C7
DDR_A_D3 A7
DDR_A_D4 B10
DDR_A_D5 D10
DDR_A_D6 E10
DDR_A_D7 A8
DDR_A_D8 D8
DDR_A_D9 F10
DDR_A_D10 E6
DDR_A_D11 SA_DQ[10]
DDR_A_D12 E9
DDR_A_D13 B7
DDR_A_D14 E7
DDR_A_D15 C6
DDR_A_D16 H10
DDR_A_D17 G8
DDR_A_D18 K7
DDR_A_D19 J8
DDR_A_D20 G7
DDR_A_D21 G10
DDR_A_D22 J7
DDR_A_D23 J10
DDR_A_D24 L7
DDR_A_D25 M6
DDR_A_D26 M8
DDR_A_D27 L9
DDR_A_D28 L6
DDR_A_D29 K8
DDR_A_D30 N8
DDR_A_D31 P9
DDR_A_D32 AH5
DDR_A_D33 AF5
DDR_A_D34 AK6
DDR_A_D35 AE6
DDR_A_D36 AE6
DDR_A_D37 AG5
DDR_A_D38 A17
DDR_A_D39 A16
DDR_A_D40 A110
DDR_A_D41 A19
DDR_A_D42 AL10
DDR_A_D43 AK12
DDR_A_D44 AK8
DDR_A_D45 AL7
DDR_A_D46 AK11
DDR_A_D47 A18
DDR_A_D48 AN8
DDR_A_D49 AM10
DDR_A_D50 AR11
DDR_A_D51 AL11
DDR_A_D52 AM9
DDR_A_D53 AN9
DDR_A_D54 AT11
DDR_A_D55 AP12
DDR_A_D56 AM12
DDR_A_D57 AN12
DDR_A_D58 AM13
DDR_A_D59 AT14
DDR_A_D60 AT12
DDR_A_D61 AL13
DDR_A_D62 AR14
DDR_A_D63 AP14

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<11> DDR_A_BS1
<11> DDR_A_BS2

<11> DDR_A_CAS#
<11> DDR_A_RAS#
<11> DDR_A_WE#

DDR SYSTEM MEMORY - A

SA_CK[0] AA6
SA_CK#0 AA7
SA_CKE[0] P7

SA_CK[1] Y6
SA_CK#1 Y6
SA_CKE[1] P6

SA_CS#0 AE2
SA_CS#1 AE8

SA_ODT[0] AD8
SA_ODT[1] AF9

SA_DM[0] B9
SA_DM[1] D7
SA_DM[2] H7
SA_DM[3] M7
SA_DM[4] AG6
SA_DM[5] AM7
SA_DM[6] AN10
SA_DM[7] AN13

SA_DQS#0 C9
SA_DQS#1 E8
SA_DQS#2 J8
SA_DQS#3 J9
SA_DQS#4 AH7
SA_DQS#5 AK9
SA_DQS#6 AP11
SA_DQS#7 AT13

SA_DQS[0] C8
SA_DQS[1] F9
SA_DQS[2] H9
SA_DQS[3] M9
SA_DQS[4] AH8
SA_DQS[5] AK10
SA_DQS[6] AN11
SA_DQS[7] AR13

SA_MA[0] Y3
SA_MA[1] W1
SA_MA[2] AA8
SA_MA[3] AA3
SA_MA[4] V1
SA_MA[5] AA9
SA_MA[6] V8
SA_MA[7] T1
SA_MA[8] Y9
SA_MA[9] U6
SA_MA[10] AD4
SA_MA[11] T2
SA_MA[12] U1
SA_MA[13] AG8
SA_MA[14] T3
SA_MA[15] V9

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DDR_A_CLK0# <11>
DDR_A_CKE0 <11>

DDR_A_CLK1 <11>
DDR_A_CLK1# <11>
DDR_A_CKE1 <11>

DDR_A_CS0# <11>
DDR_A_CS1# <11>

DDR_A_ODT0 <11>
DDR_A_ODT1 <11>

DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7

DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7

DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7

DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_MA15

IC:AUB_CFD_rPGA,R0P9
CONN@

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<12> DDR_B_DQS#0[0..7]
<12> DDR_B_DQS#0[0..7]
<12> DDR_B_MA[0..15]

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DDR_B_D2 C3
DDR_B_D3 B3
DDR_B_D4 E4
DDR_B_D5 A6
DDR_B_D6 C4
DDR_B_D7 D1
DDR_B_D8 D2
DDR_B_D9 D2
DDR_B_D10 F2
DDR_B_D11 E1
DDR_B_D12 C2
DDR_B_D13 E5
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DDR_B_D15 G4
DDR_B_D16 H6
DDR_B_D17 G2
DDR_B_D18 J6
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DDR_B_D25 K2
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DDR_B_D27 M1
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DDR_B_D36 AG4
DDR_B_D37 AG3
DDR_B_D38 AJ4
DDR_B_D39 AH4
DDR_B_D40 AK4
DDR_B_D41 AK3
DDR_B_D42 AM6
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DDR_B_D48 AP3
DDR_B_D49 AN5
DDR_B_D50 AT4
DDR_B_D51 AN6
DDR_B_D52 AN4
DDR_B_D53 AN3
DDR_B_D54 AT5
DDR_B_D55 AT6
DDR_B_D56 AN7
DDR_B_D57 AP6
DDR_B_D58 AP8
DDR_B_D59 AT9
DDR_B_D60 AT7
DDR_B_D61 AP9
DDR_B_D62 AR10
DDR_B_D63 AT10

SB_DQ[0] B5
SB_DQ[1] A5
SB_DQ[2] C3
SB_DQ[3] B3
SB_DQ[4] E4
SB_DQ[5] A6
SB_DQ[6] C4
SB_DQ[7] D1
SB_DQ[8] D2
SB_DQ[9] D2
SB_DQ[10] F2
SB_DQ[11] E1
SB_DQ[12] C2
SB_DQ[13] E5
SB_DQ[14] F3
SB_DQ[15] G4
SB_DQ[16] H6
SB_DQ[17] G2
SB_DQ[18] J6
SB_DQ[19] J3
SB_DQ[20] G5
SB_DQ[21] G5
SB_DQ[22] J2
SB_DQ[23] J1
SB_DQ[24] J5
SB_DQ[25] K2
SB_DQ[26] L3
SB_DQ[27] M1
SB_DQ[28] K5
SB_DQ[29] K4
SB_DQ[30] M4
SB_DQ[31] N5
SB_DQ[32] AE1
SB_DQ[33] AG1
SB_DQ[34] AJ3
SB_DQ[35] AK1
SB_DQ[36] AG4
SB_DQ[37] AG3
SB_DQ[38] AJ4
SB_DQ[39] AH4
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SB_DQ[41] AK3
SB_DQ[42] AM6
SB_DQ[43] AN2
SB_DQ[44] AK5
SB_DQ[45] AK2
SB_DQ[46] AM4
SB_DQ[47] AM3
SB_DQ[48] AP3
SB_DQ[49] AN5
SB_DQ[50] AT4
SB_DQ[51] AN6
SB_DQ[52] AN4
SB_DQ[53] AN3
SB_DQ[54] AT5
SB_DQ[55] AT6
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SB_DQ[59] AT9
SB_DQ[60] AT7
SB_DQ[61] AP9
SB_DQ[62] AR10
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<12> DDR_B_RAS#
<12> DDR_B_WE#

JCPU1D

DDR SYSTEM MEMORY - B

SB_CK[0] W8
SB_CK#0 W9
SB_CKE[0] M3

SB_CK[1] V7
SB_CK#1 V6
SB_CKE[1] M2

SB_CS#0 AB8
SB_CS#1 AD6

SB_ODT[0] AC7
SB_ODT[1] AD1

SB_DM[0] D4
SB_DM[1] E1
SB_DM[2] H3
SB_DM[3] K1
SB_DM[4] AH1
SB_DM[5] AL2
SB_DM[6] AR4
SB_DM[7] AT8

SB_DQS#0 D5
SB_DQS#1 E4
SB_DQS#2 D4
SB_DQS#3 D4
SB_DQS#4 AH2
SB_DQS#5 AL4
SB_DQS#6 AR5
SB_DQS#7 AR8

SB_DQS[0] C5
SB_DQS[1] E3
SB_DQS[2] H4
SB_DQS[3] M5
SB_DQS[4] AG2
SB_DQS[5] AL5
SB_DQS[6] AP5
SB_DQS[7] AR7

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SB_MA[1] V2
SB_MA[2] T5
SB_MA[3] V3
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SB_MA[7] R6
SB_MA[8] R4
SB_MA[9] R5
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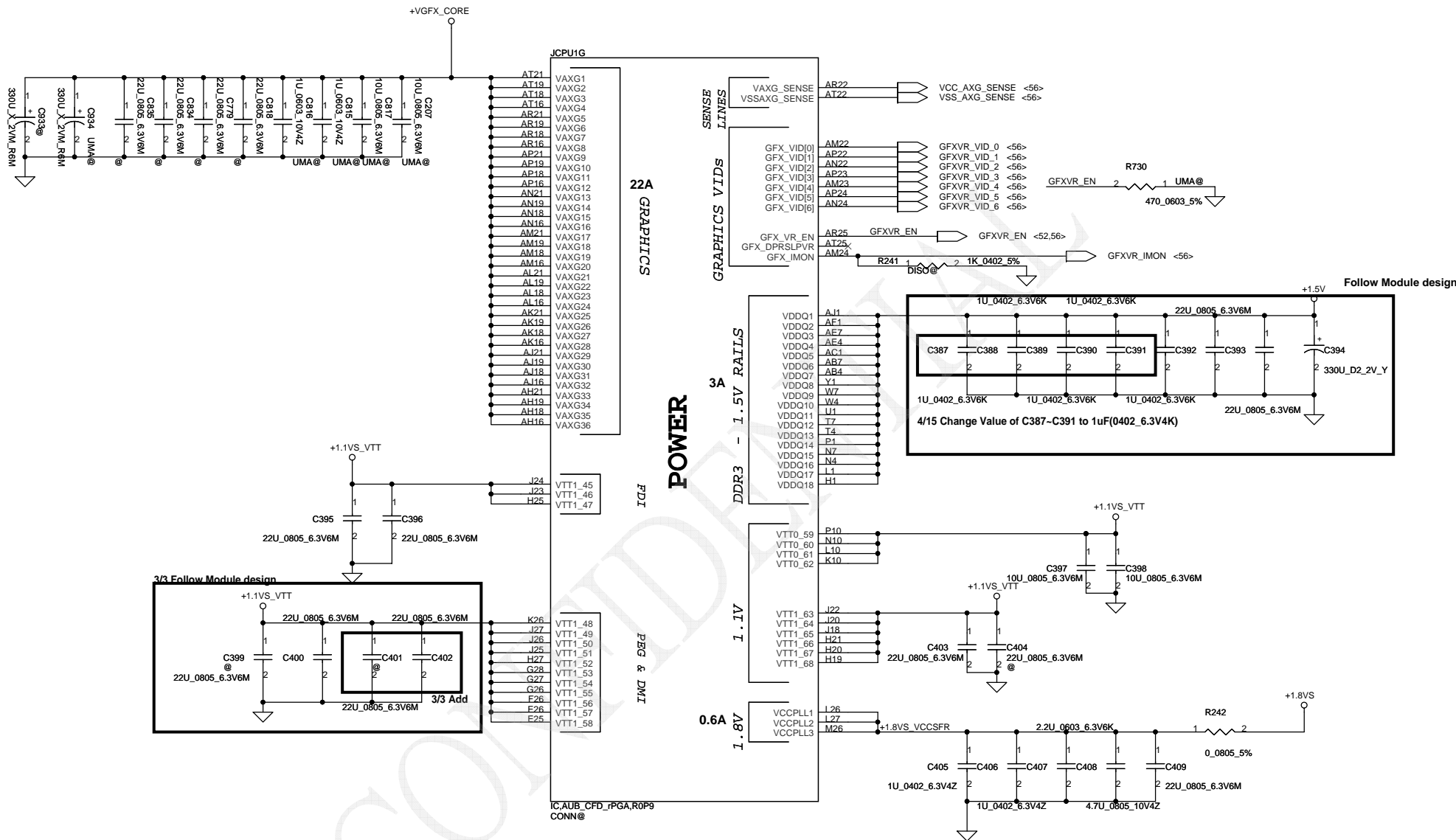
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DDR_B_DQS#6
DDR_B_DQS#7

DDR_B_DQS0
DDR_B_DQS1
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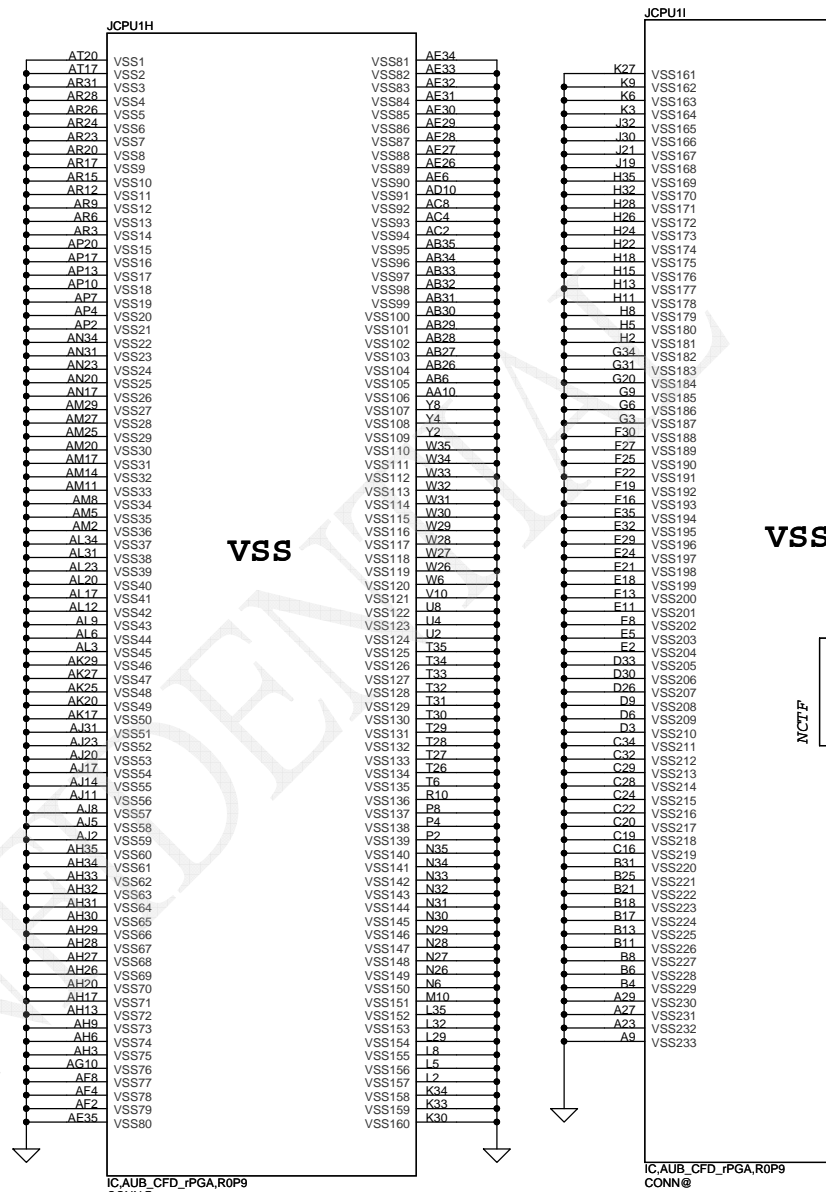
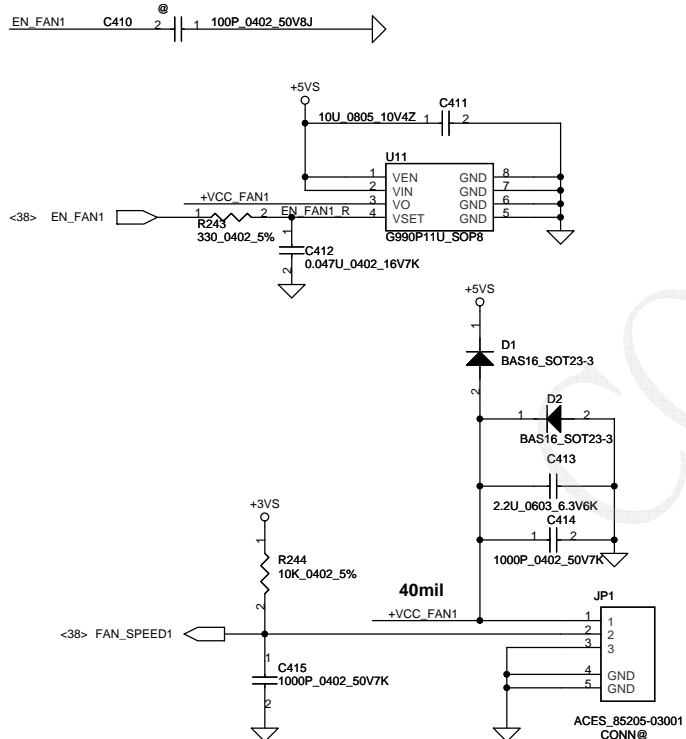
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CONN@

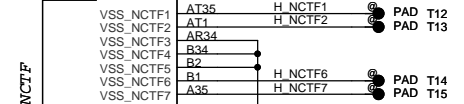
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FAN1 Conn



VSS

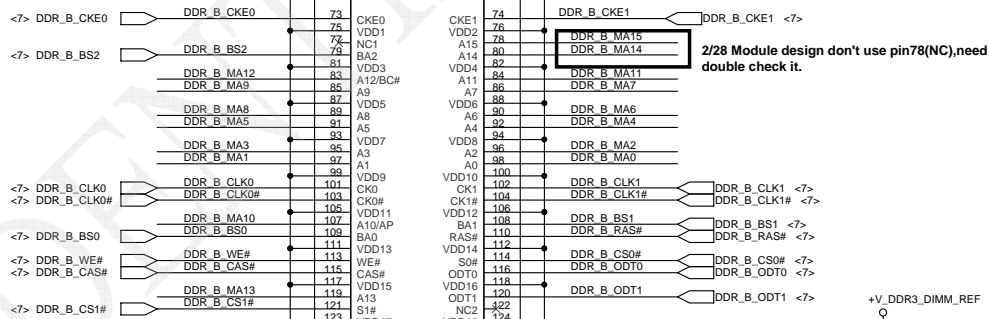
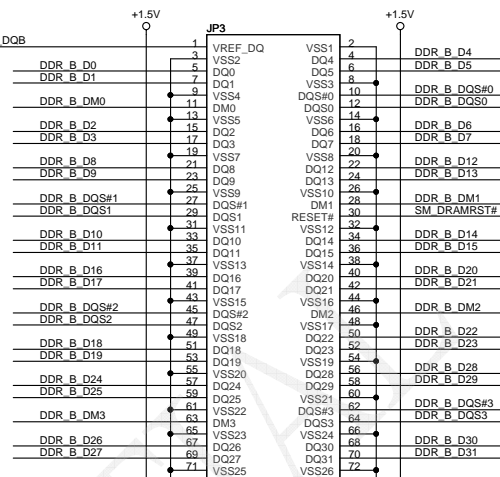
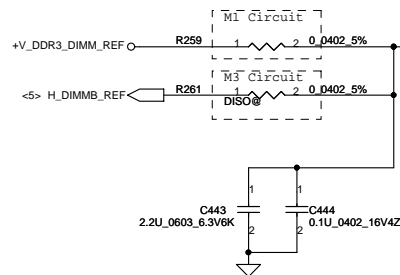


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Rev	B
				Date:	Thursday, June 10, 2010
				Sheet	10 of 59

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Issued Date	2009/02/04	Deciphered Date	2010/02/04	Title	SCHEMATIC, MB A6001	
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				401839	401839	B
				Date:	Thursday, June 10, 2010	Sheet 11 of 59

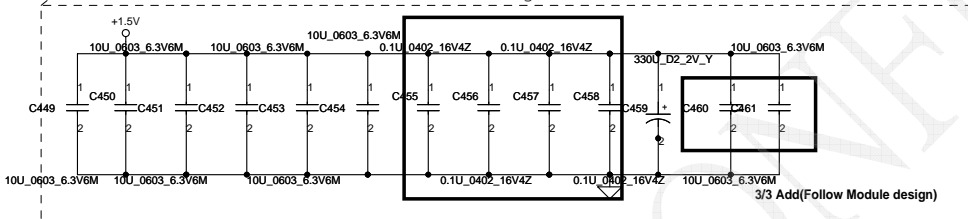
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2008/9/8 #400755
Calpella Clarksfeld
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details



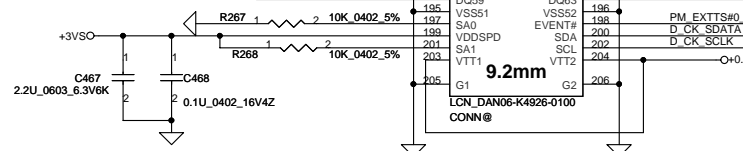
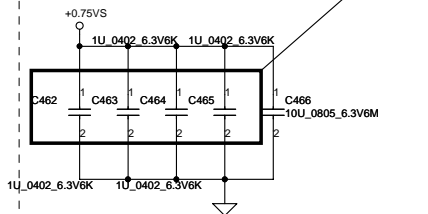
Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



Layout Note:
Place near JP3.203 & JP3.204

4/15 Change value of C462-C465 from
1uF(0603_10V4Z) to 1U(0402_6.3V6K)
Follow Module design



DDR3 SO-DIMM B
Standard Type

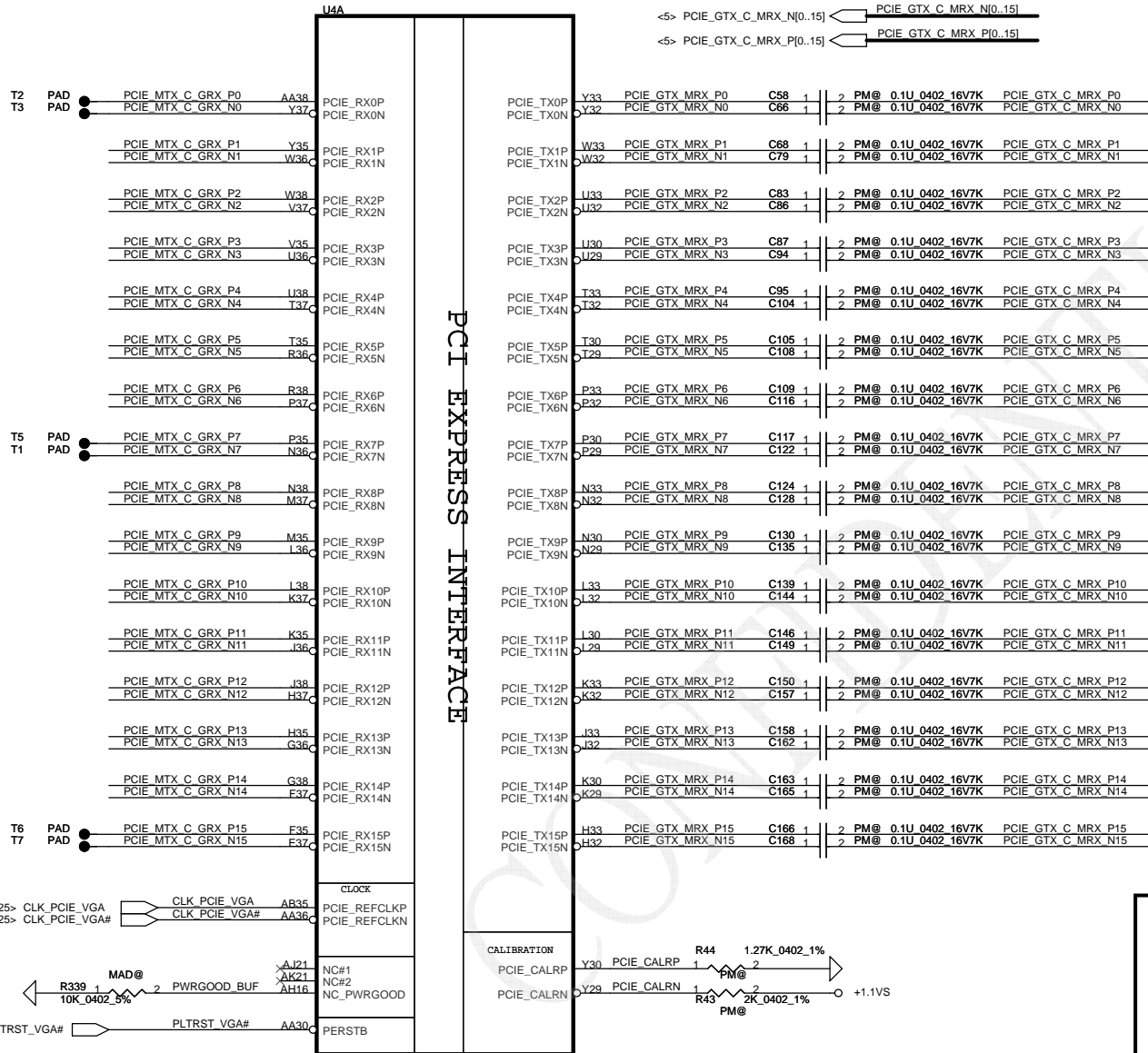
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Issued Date	2009/02/04	Deciphered Date	2010/02/04	Compal Electronics, Inc.	
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				401839	
				Date: Thursday, June 10, 2010	Sheet 12 of 59

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216-0729042 A13 M96-M2 FCBGA962 0FA
M96@

U4
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216-0772000 A11 MADISON PRO 030
MADVGA@

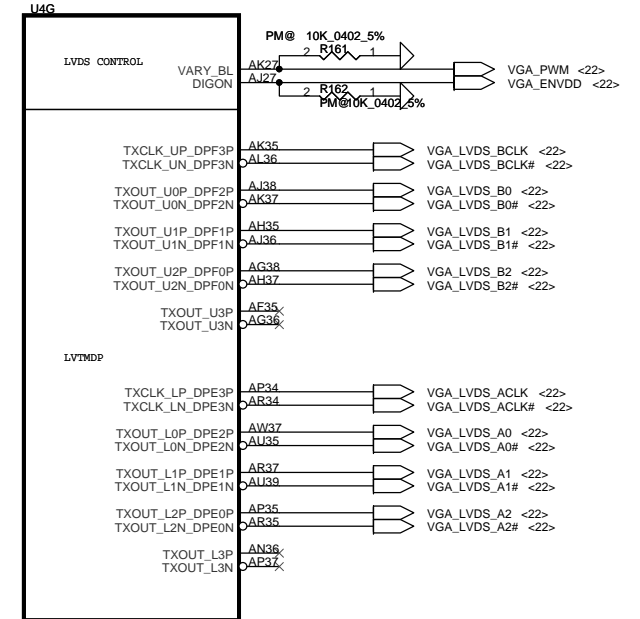
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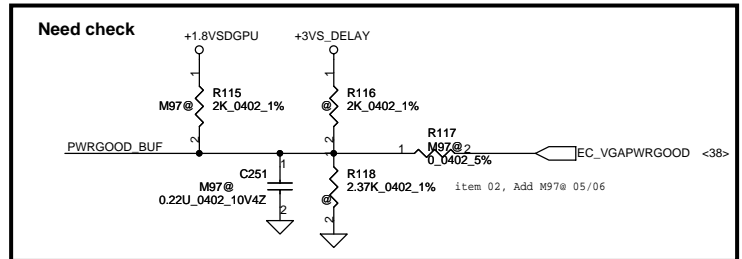


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the same with M86

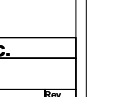
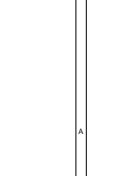
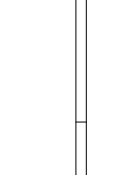
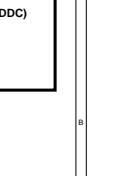
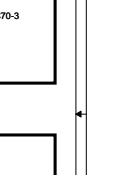
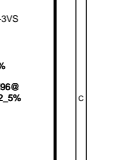
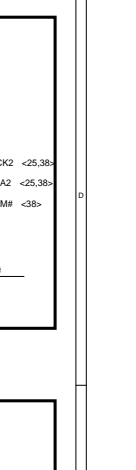
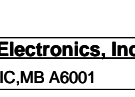
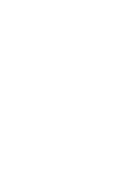
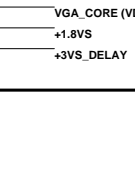
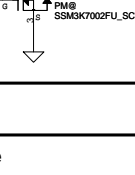
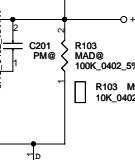
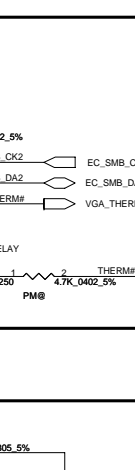
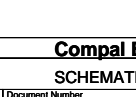
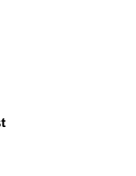
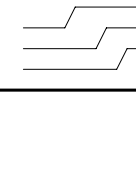
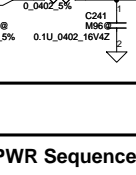
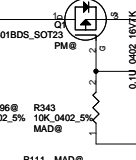
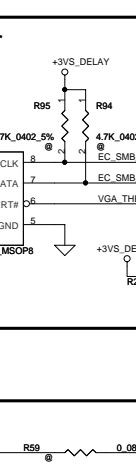
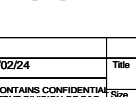
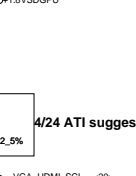
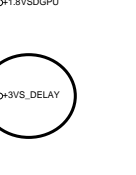
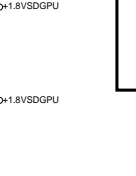
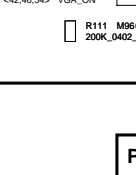
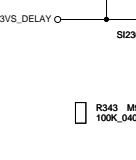
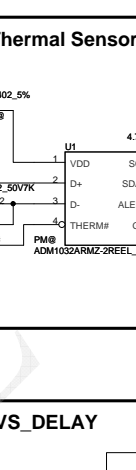
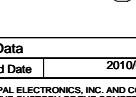
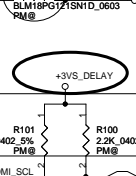
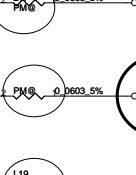
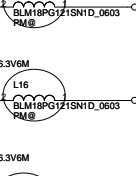
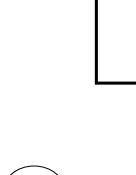
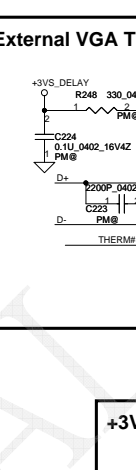
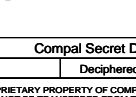
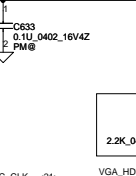
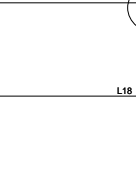
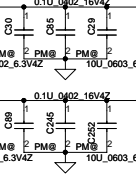
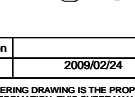
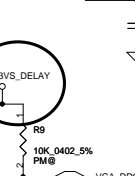
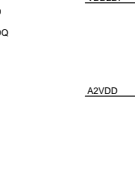
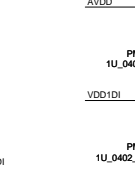
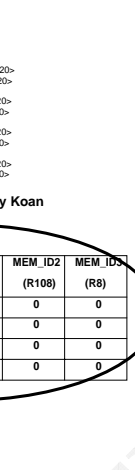
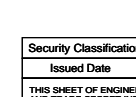
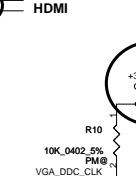
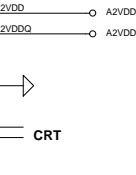
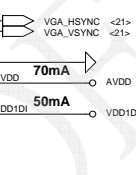
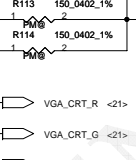
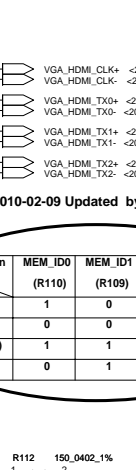
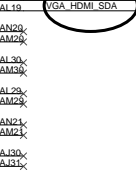
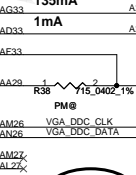
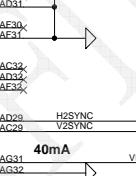
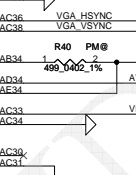
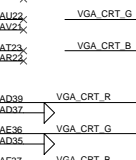
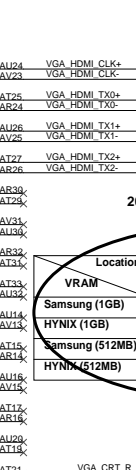
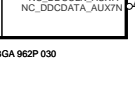
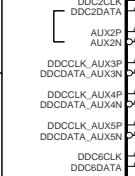
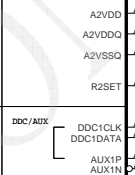
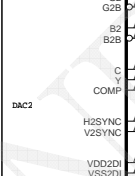
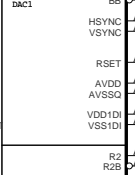
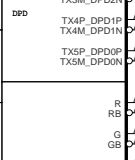
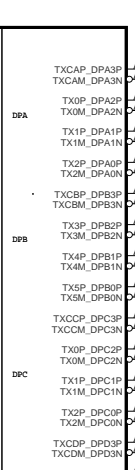
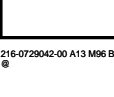
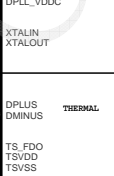
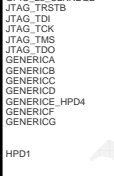
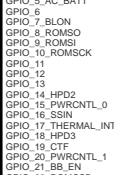
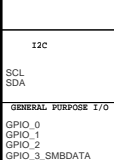
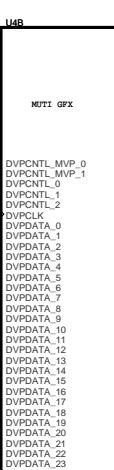
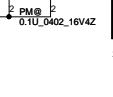
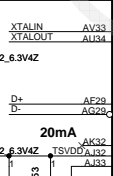
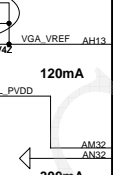
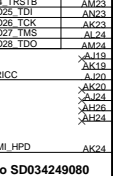
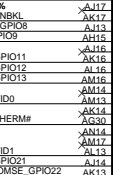
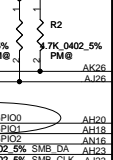
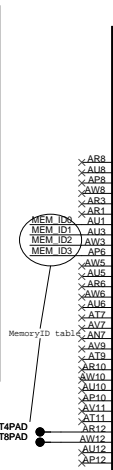
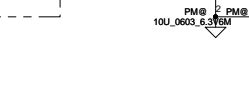
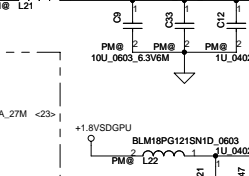
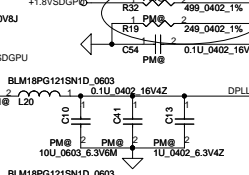
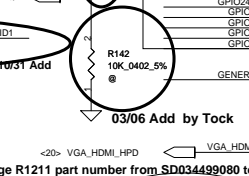
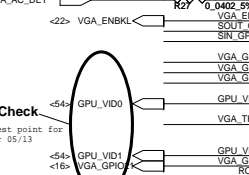
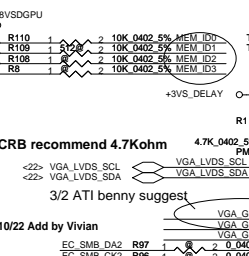
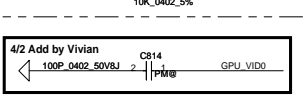
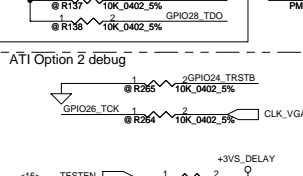
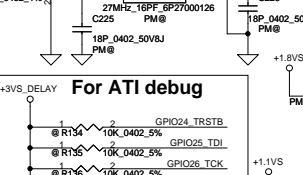
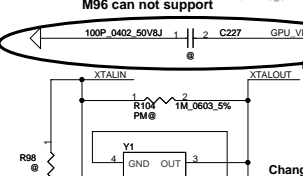
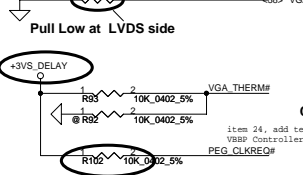
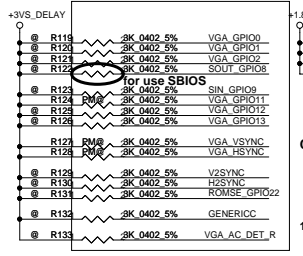


216-0729042-00 A13 M96 BGA 962P 030
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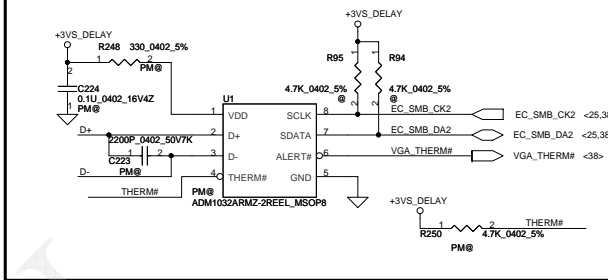


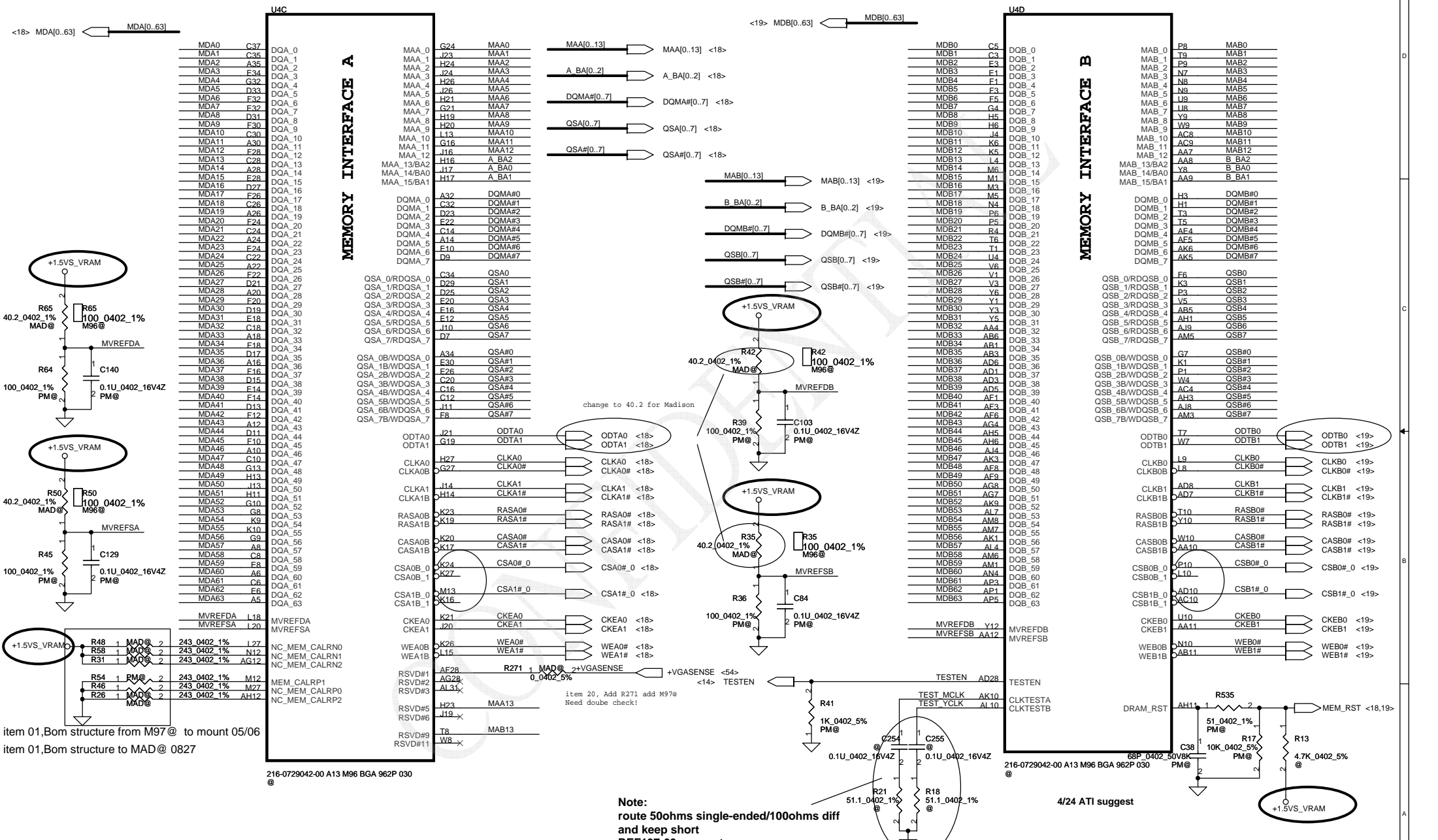
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Strap Name	Pin Straps description	Default Value
TX_PWRS_EN#	GPIO0 Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN#	GPIO1 PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2 0: Advertises the PCI-E device as 2.5 GT/s capable at power-on 1: Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
	GPIO23 GPIO21 Reserved	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type 128 MB 000 256 MB 001 64 MB 010 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 02: Audio for both DisplayPort and HDMI	1
	GENERICC H2SYNC Reserved	0
VIP_DEVICE STRAP_EN	V2SYNC Reserved	0

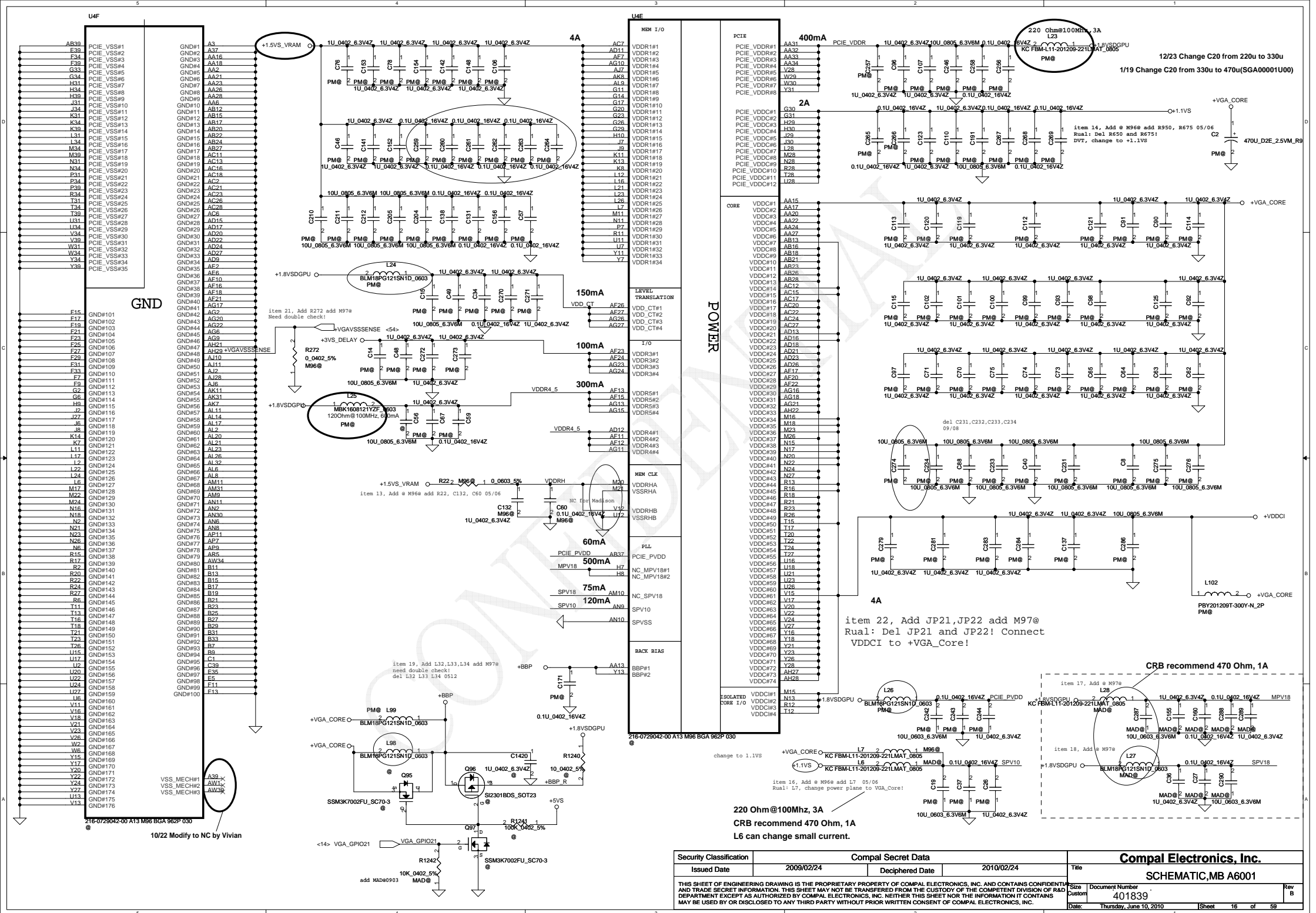


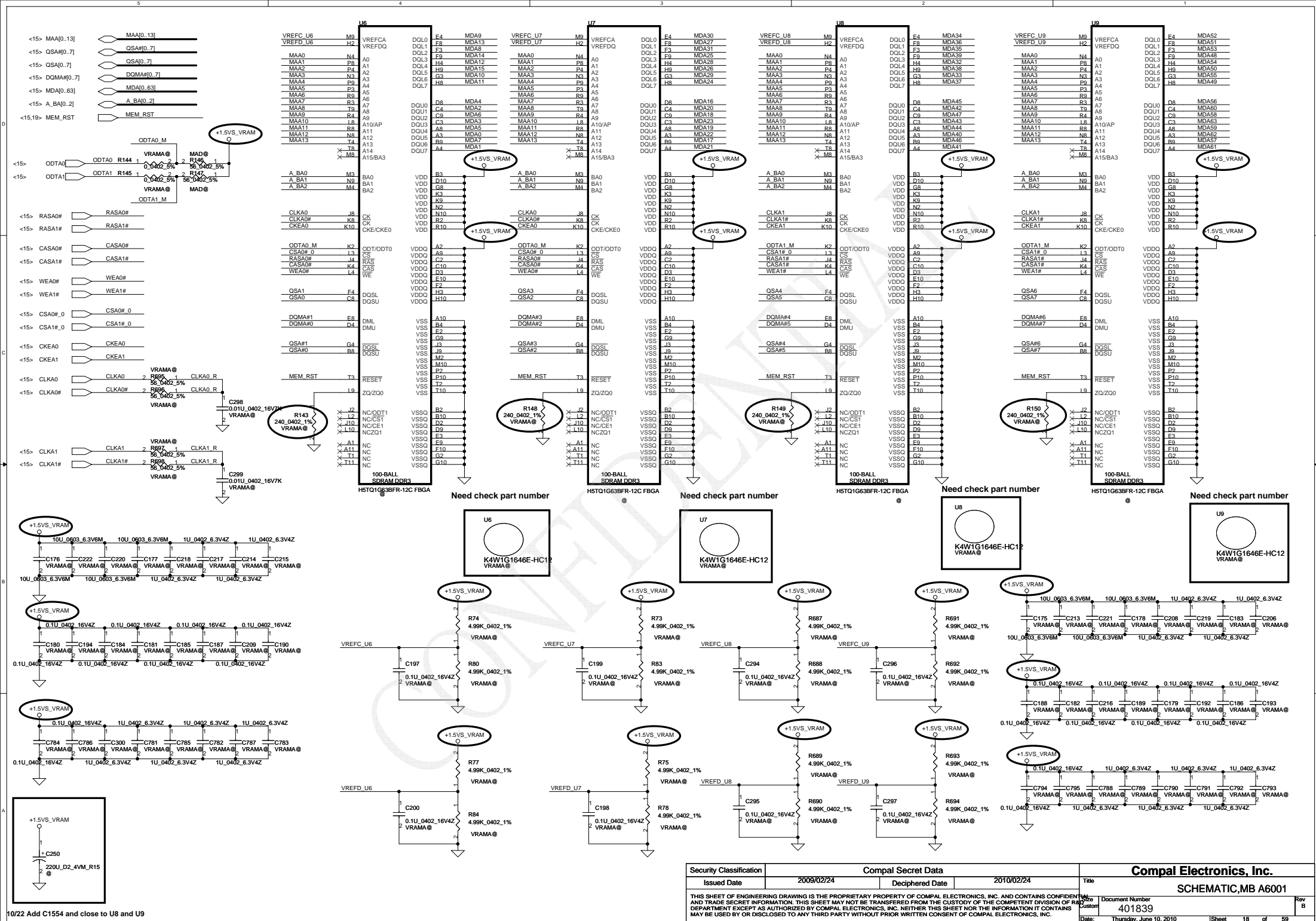
External VGA Thermal Sensor

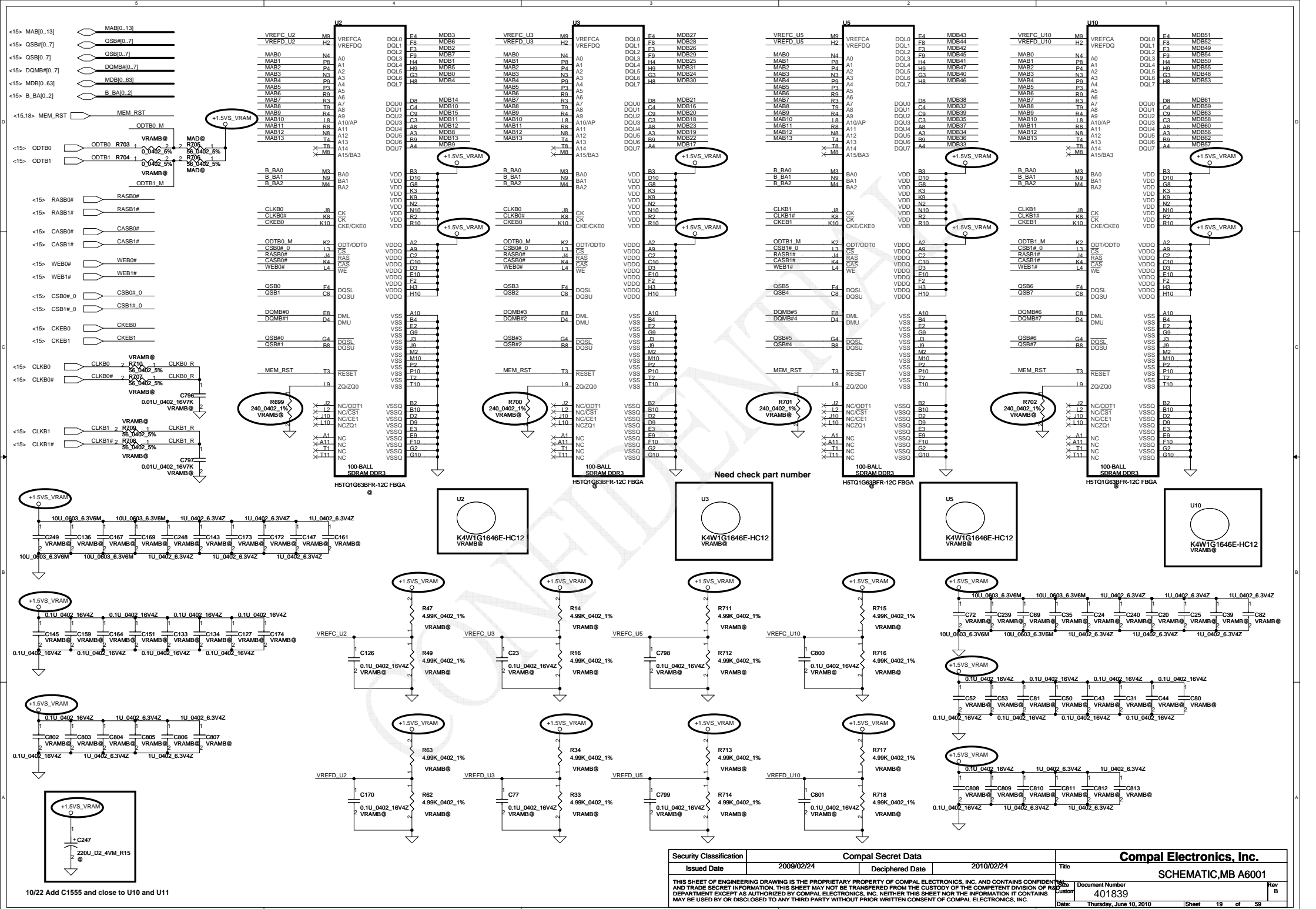




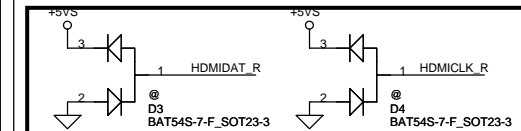
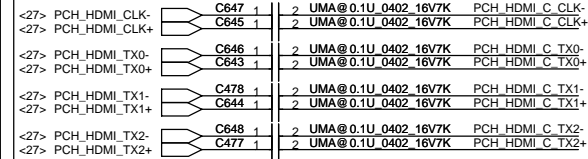
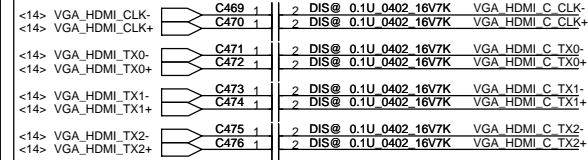
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						Custom		401839		B	
						Date:		Thursday, June 10, 2010		Sheet 15 of 59	



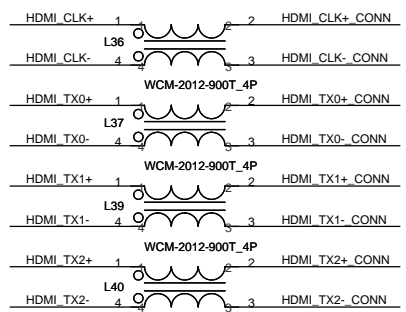
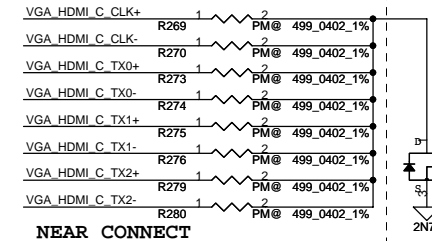




have the pull high on PCH/VGA side

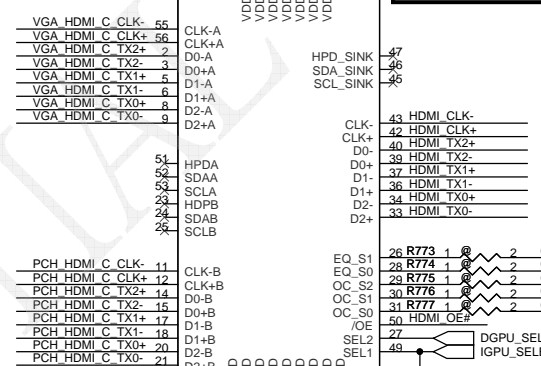
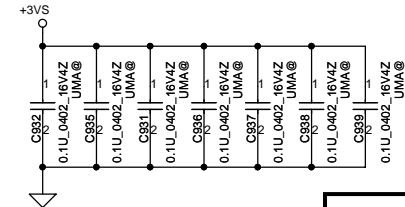
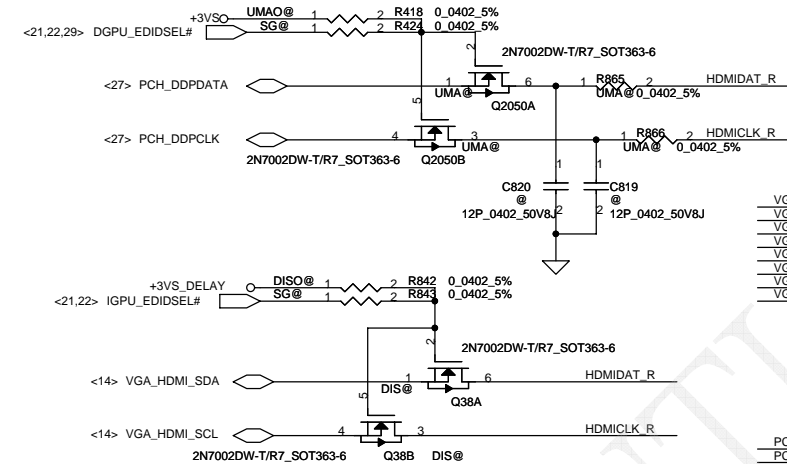
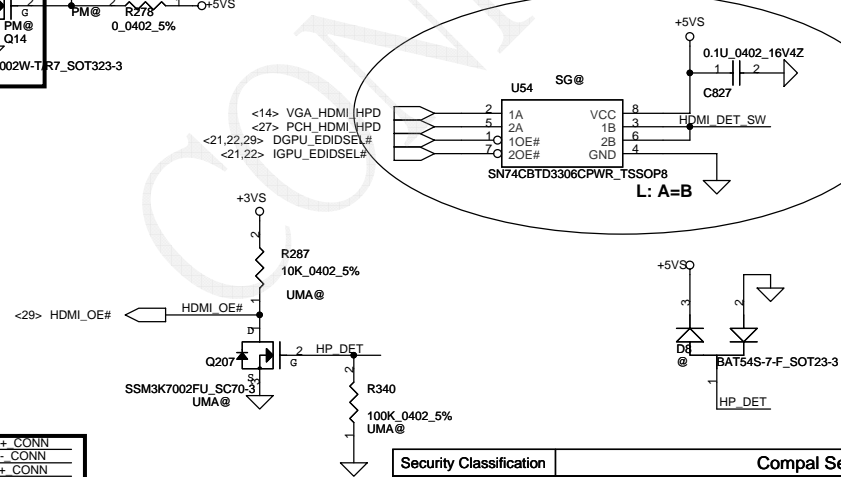
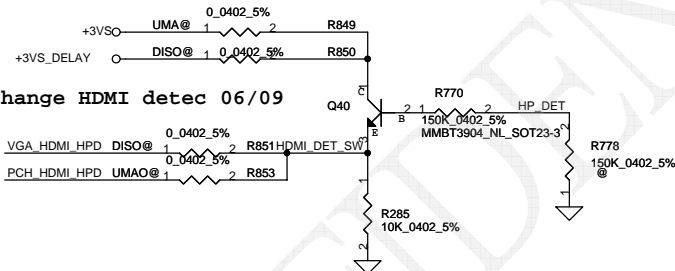


TMDs pull down (500ohm) resistors G9x only



HDMI_CLK+	@ R288	1	2	0.0402_5%	HDMI_CLK+ CONN
HDMI_CLK-	@ R289	1	2	0.0402_5%	HDMI_CLK- CONN
HDMI_TX0+	@ R290	1	2	0.0402_5%	HDMI_TX0+ CONN
HDMI_TX0-	@ R291	1	2	0.0402_5%	HDMI_TX0- CONN
HDMI_TX1+	@ R292	1	2	0.0402_5%	HDMI_TX1+ CONN
HDMI_TX1-	@ R293	1	2	0.0402_5%	HDMI_TX1- CONN
HDMI_TX2+	@ R294	1	2	0.0402_5%	HDMI_TX2+ CONN
HDMI_TX2-	@ R295	1	2	0.0402_5%	HDMI_TX2- CONN

DVT, change HDMI detec 06/09

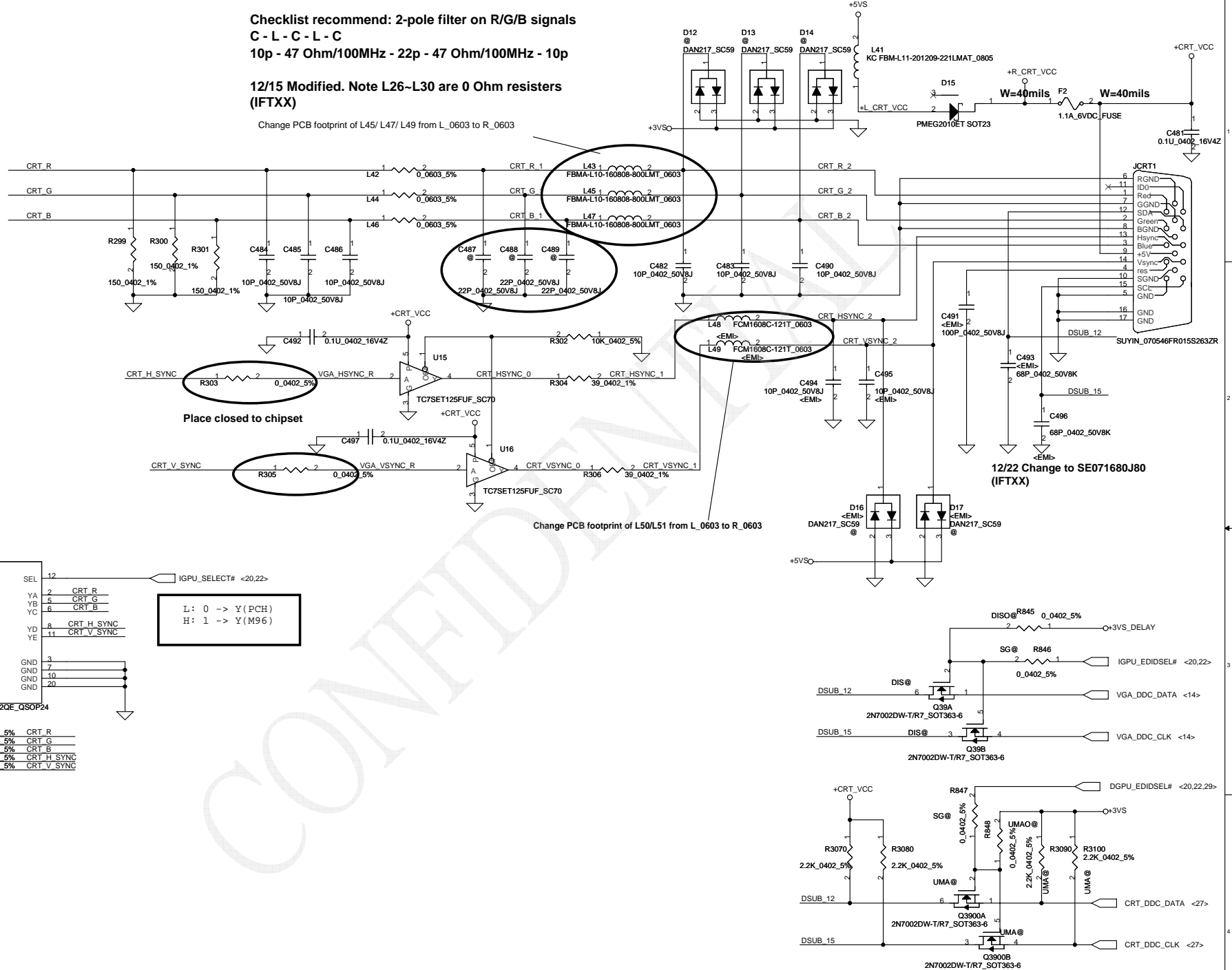


CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

12/15 Modified. Note L26~L30 are 0 Ohm resistors (IFTXX)

Change PCB footprint of L45/ L47/ L49 from L_0603 to R_0603



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10K 0402 5% 1 2 R311

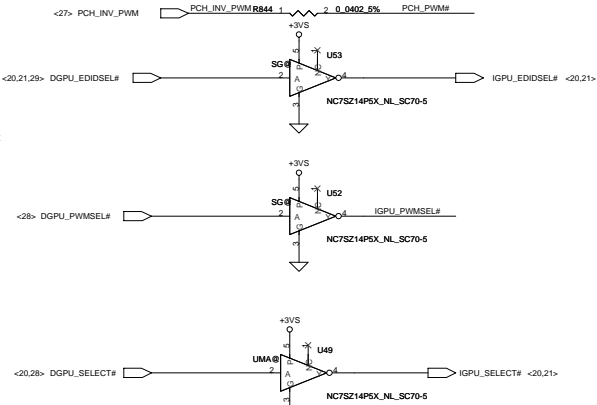
100P 0402 50V8J 1 2 C498 BKOFF#

100P 0402 50V8J 1 2 C879 VGA_ENVDD

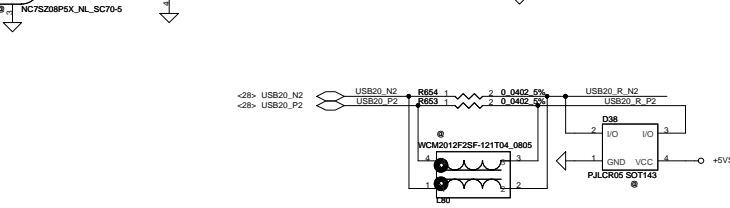
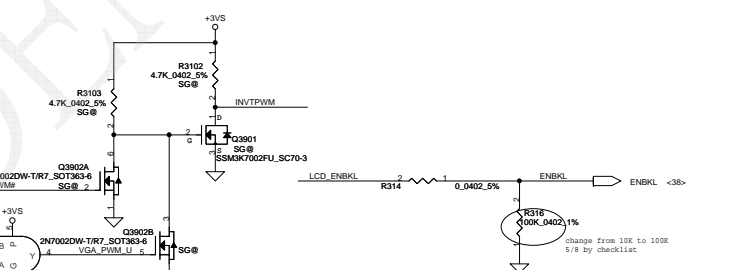
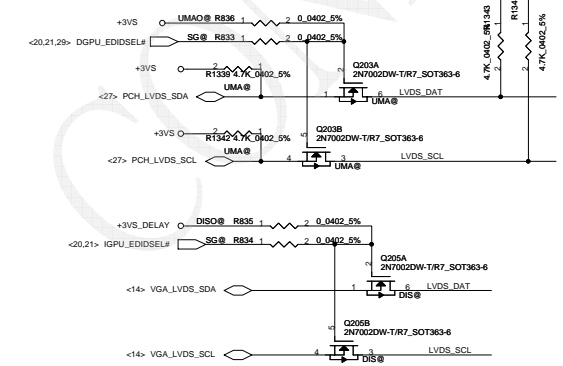
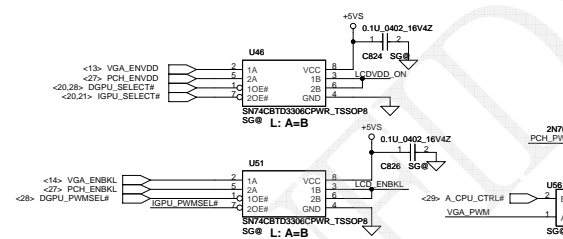
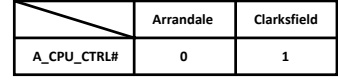
470P 0402 50V7K 1 2 C501 INTPWM

470P 0402 50V7K 1 2 C503 BKOFF#

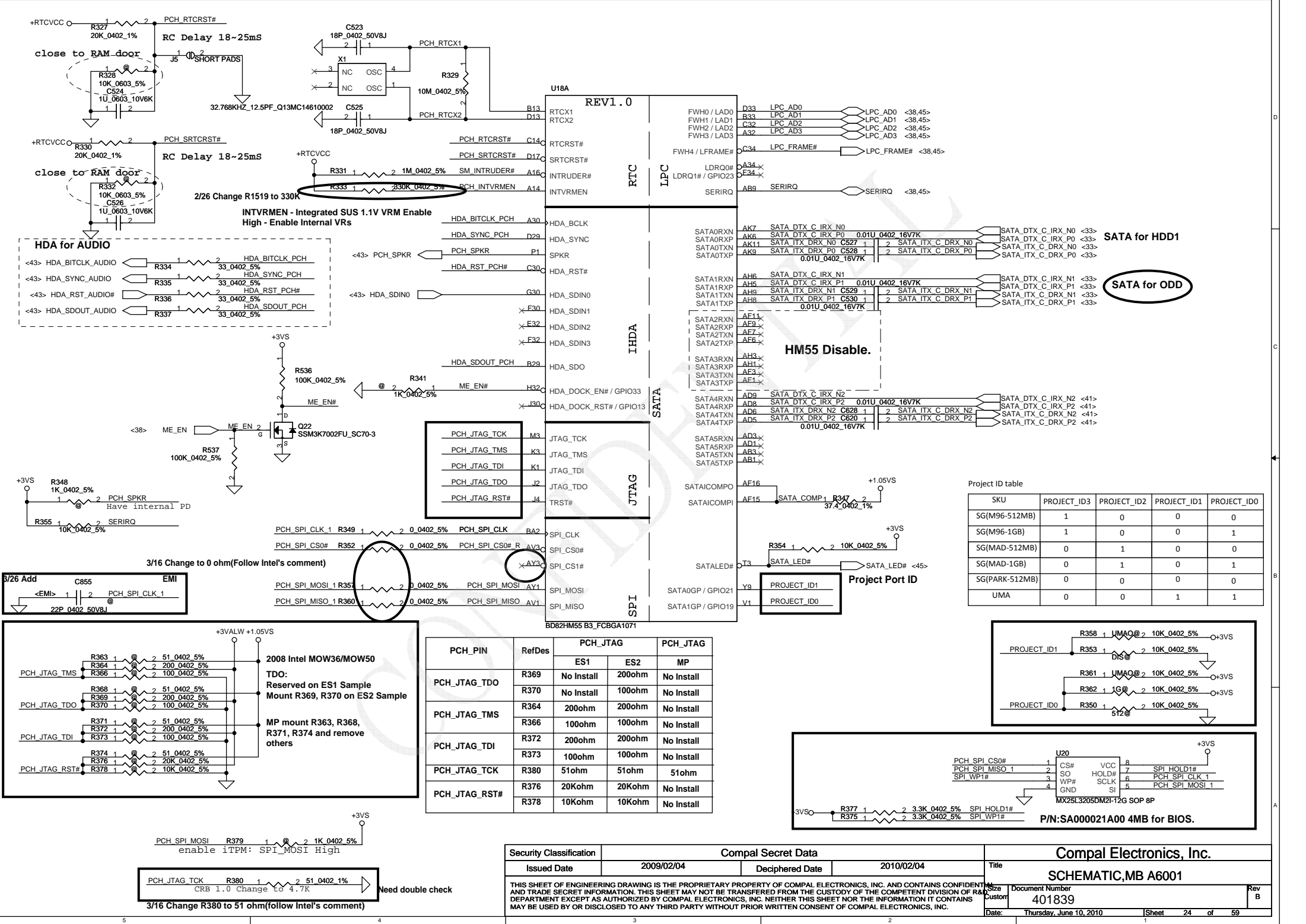
0.1U 0402 16V4Z 2 C509 +LCDVDD CONN



U45



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For Wireless LAN

For PCIE LAN

For Wireless LAN

For PCIE LAN

REV1.0

PCI-E*

From CLK BUFFER

Clock Flex

Project ID		
ID1	ID0	Project
0	0	Future
0	1	JV

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1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

3/16 Add by Vivian(follow Intel's comment)

2/28 Follow Module design Rev1.0

Buffer Mode check is need or not

3/20 Remove by Vivian

3/16 Change R408/R409 to 2.2K ohm(follow Intel's comment)

3/16 Add R761/R762 to 2.2K ohm(follow Intel's comment)

2008/1/6 2009MOW01 change to 22 ohm

<5> DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
<5> DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
<5> DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
<5> DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

U18C

REV1.0

DMI HTX PRX N0 BC24
DMI HTX PRX N1 BJ22
DMI HTX PRX N2 AW20
DMI HTX PRX N3 BJ20
DMI HTX PRX P0 BD24
DMI HTX PRX P1 BG22
DMI HTX PRX P2 BA20
DMI HTX PRX P3 BG20
DMI PTX HRX N0 BE22
DMI PTX HRX N1 BF21
DMI PTX HRX N2 BD20
DMI PTX HRX N3 BE18
DMI PTX HRX P0 BD22
DMI PTX HRX P1 BH21
DMI PTX HRX P2 BC20
DMI PTX HRX P3 BD18

DMIORXN
DMI1RXN
DMI2RXN
DMI3RXN
DMIORXP
DMI1RXP
DMI2RXP
DMI3RXP
DMIOTXN
DMI1TXN
DMI2TXN
DMI3TXN
DMIOTXP
DMI1TXP
DMI2TXP
DMI3TXP

FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7

BA18 FDI CTX PRX N0
BH17 FDI CTX PRX N1
BD16 FDI CTX PRX N2
BJ16 FDI CTX PRX N3
BA16 FDI CTX PRX N4
BE14 FDI CTX PRX N5
BA14 FDI CTX PRX N6
BC12 FDI CTX PRX N7
BB18 FDI CTX PRX P0
BE17 FDI CTX PRX P1
BC16 FDI CTX PRX P2
BG16 FDI CTX PRX P3
AW16 FDI CTX PRX P4
BD14 FDI CTX PRX P5
BB14 FDI CTX PRX P6
BD12 FDI CTX PRX P7

08/20 ADD
FDI for SG

FDI_CTX_PRX_N[0..7] <5>
FDI_CTX_PRX_P[0..7] <5>

FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

BJ14 FDI_INT
BE13 FDI_FSYNC0
BH13 FDI_FSYNC1
BJ12 FDI_LSYNC0
BG14 FDI_LSYNC1

FDI_INT <5>
FDI_FSYNC0 <5>
FDI_FSYNC1 <5>
FDI_LSYNC0 <5>
FDI_LSYNC1 <5>

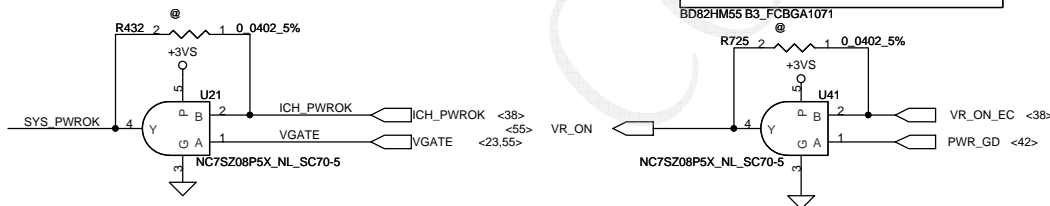
System Power Management

<6> XDP_DBRESET# XDP_DBRESET# T6
SYS_PWROK R426 2 1 0 0402 5% SYS_PWROK R M6
VGATE R427 2 1 0 0402 5%
SYS_PWROK B17
MEPWROK K5
LAN_RST# A10
LAN_RST# D9
DRAMPWROK C16
PCH_RSMRST# M1
SUS_PWR_ACK M1
PBTN_OUT# P5
PCH_ACIN P7
PCH_GPIO72 A6
EC_SWI# F14

SYS_RESET#
WAKE#
CLKRUN# / GPIO32
PWROK
SUS_STAT# / GPIO61
SUSCLK / GPIO62
SLP_S5# / GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN# / GPIO29

PCH_PCIE_WAKE# <35,37>
PM_CLKRUN# <38,45>
SUS_STAT# <45>
SUSCLK <38>
PM_SLP_S5# <38>
PM_SLP_S4# <38>
PM_SLP_S3# <38>
PM_SLP_M# @ PAD T19
PM_SLP_DS# @ PAD T20
H_PM_SYNC <6>
PM_SLP_LAN#

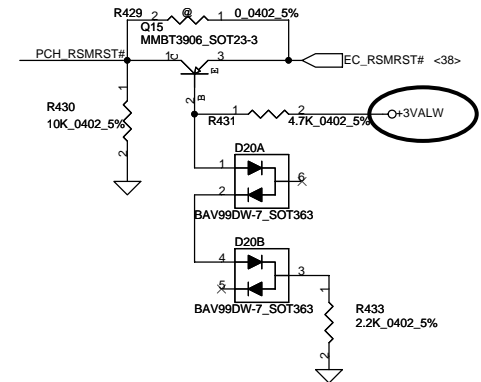
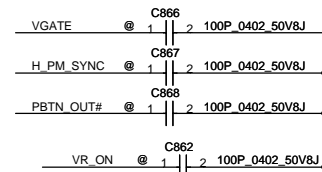
10/2 Intel suggestion change to 10K
CH751H-40PT_SOD323-2



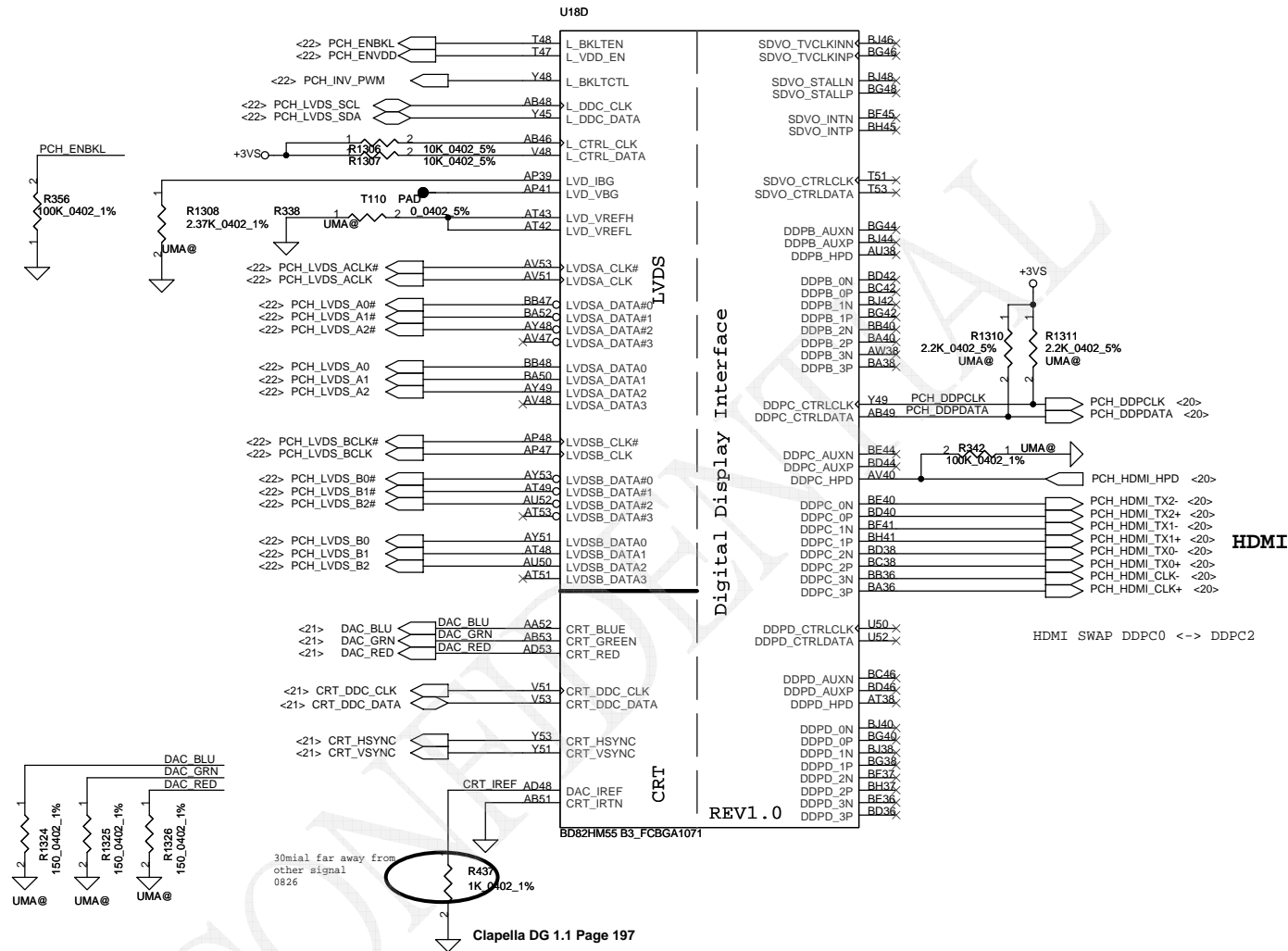
SYS_PWROK R434 10K_0402_5%
ICH_PWROK R435 10K_0402_5%
LAN_RST# R436 10K_0402_5%

No used Integrated LAN,
connecting LAN_RST# to GND

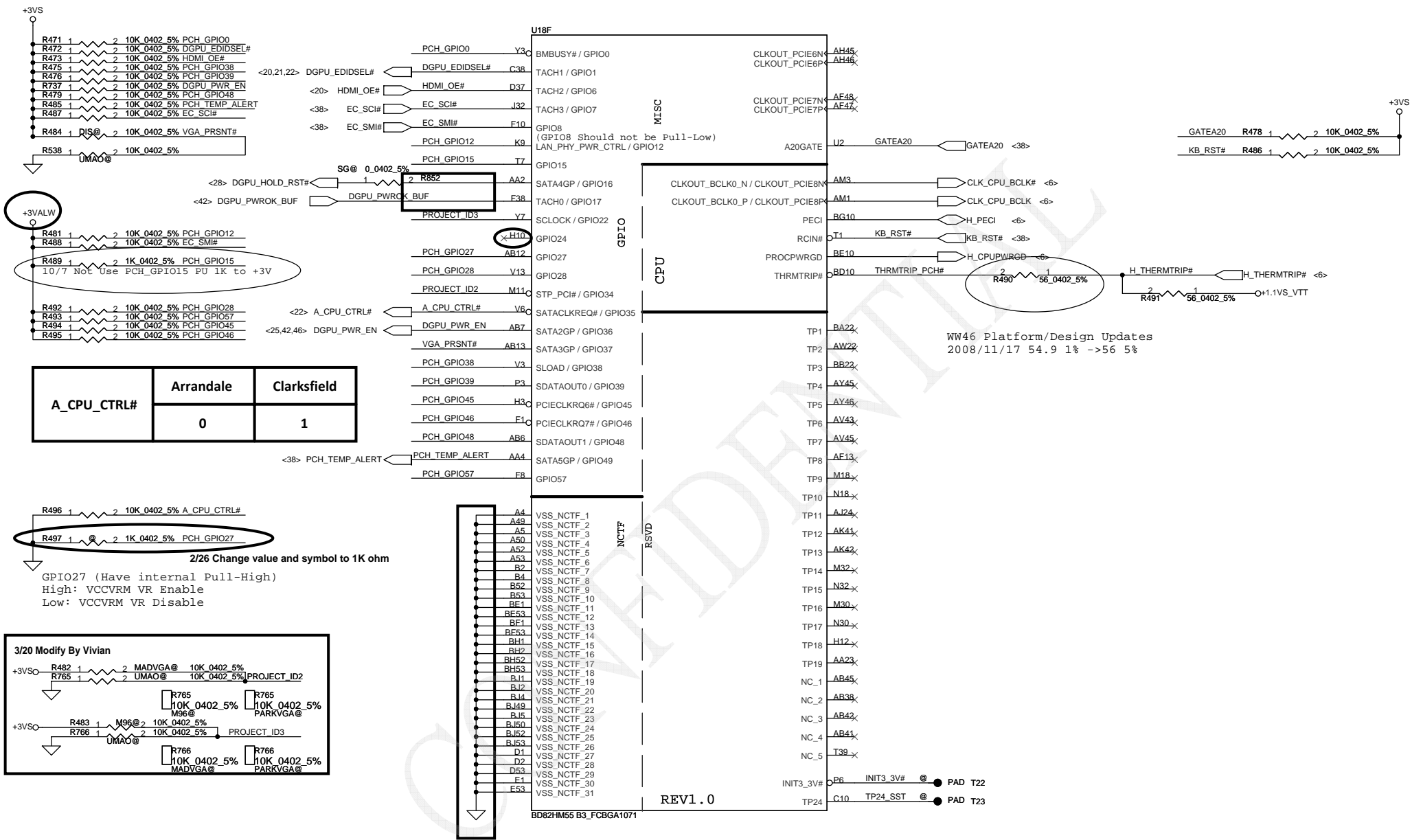
4/2 Add by Vivian

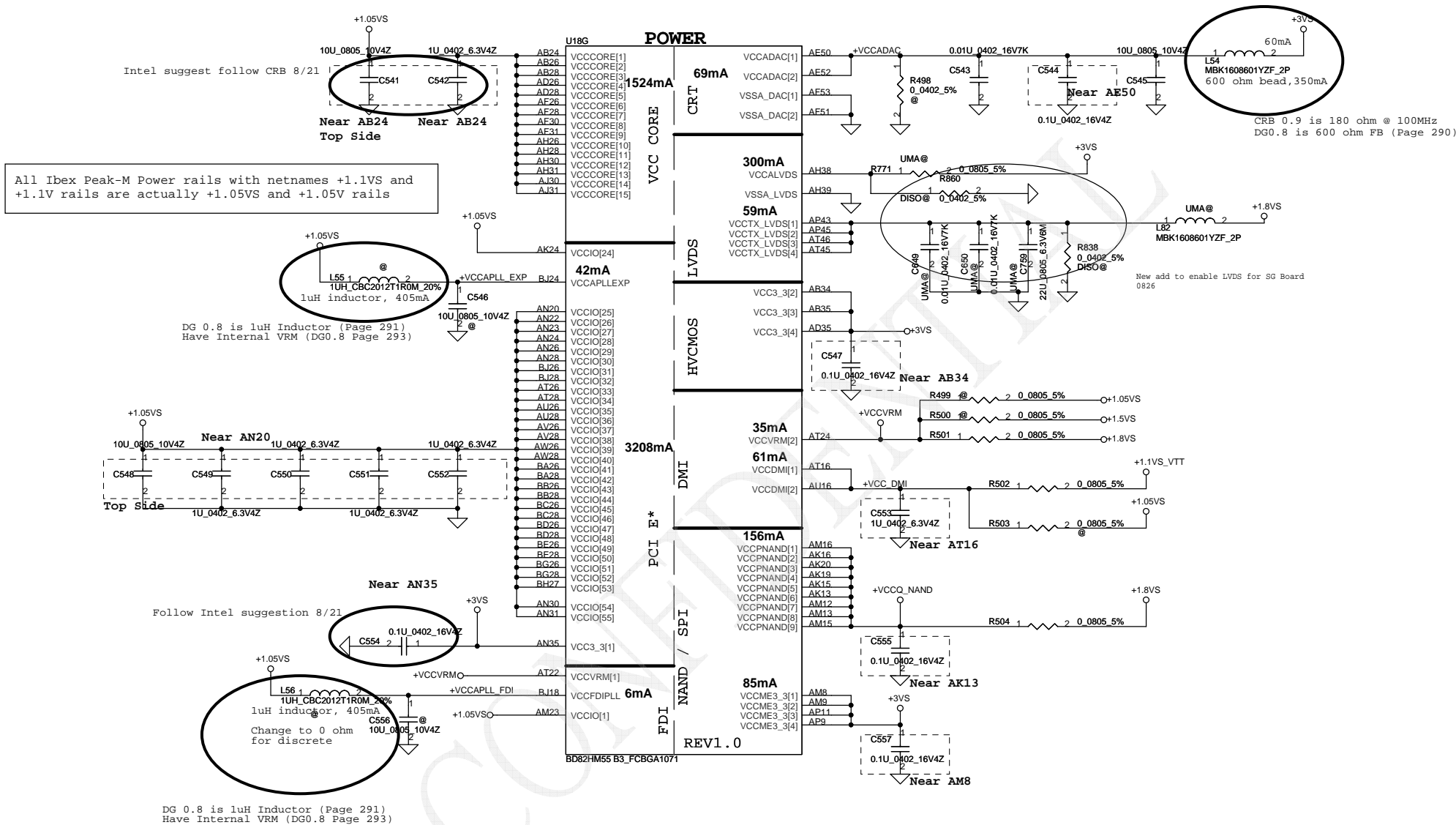


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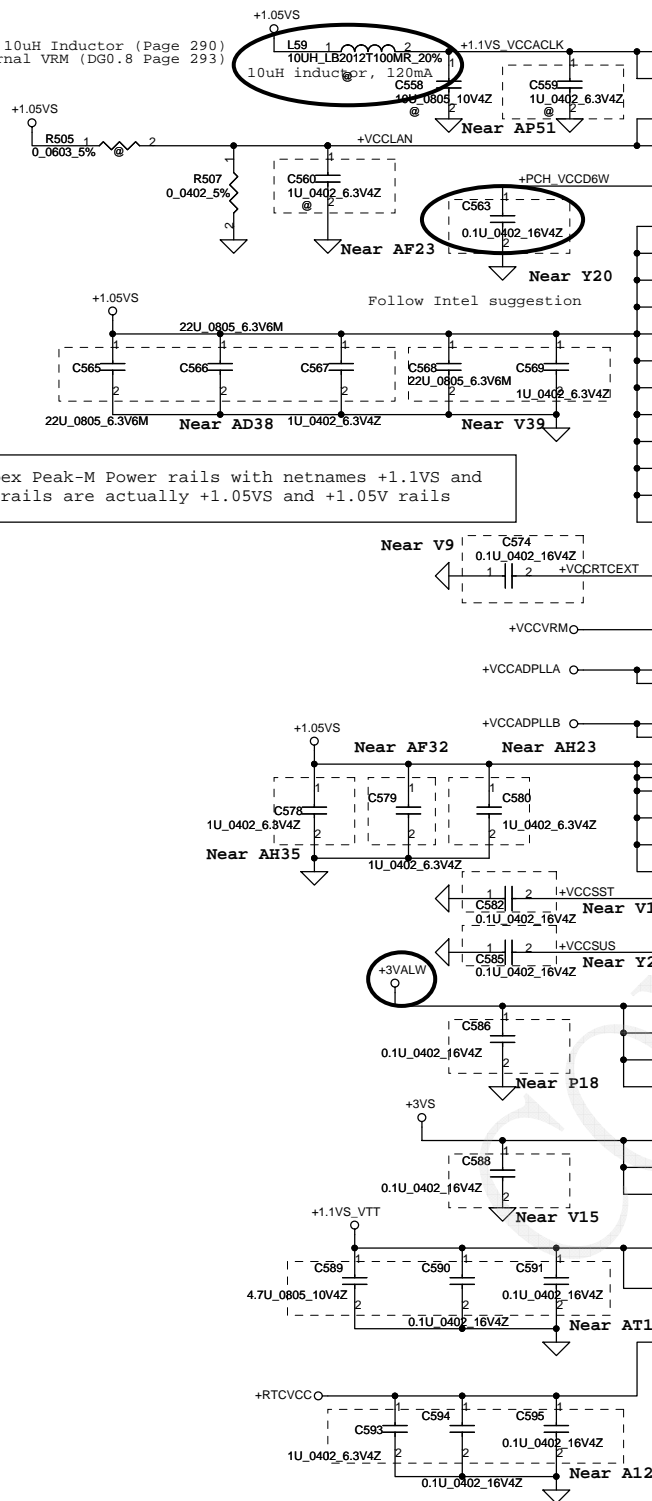
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DG 0.8 is 10uH Inductor (Page 290)
Have Internal VRM (DG0.8 Page 293)



All Ixbox Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

POWER

REV1.0

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

PCI/GPIO/LPC

CPU

RTC

HDA

Security Classification

Compal Secret Data

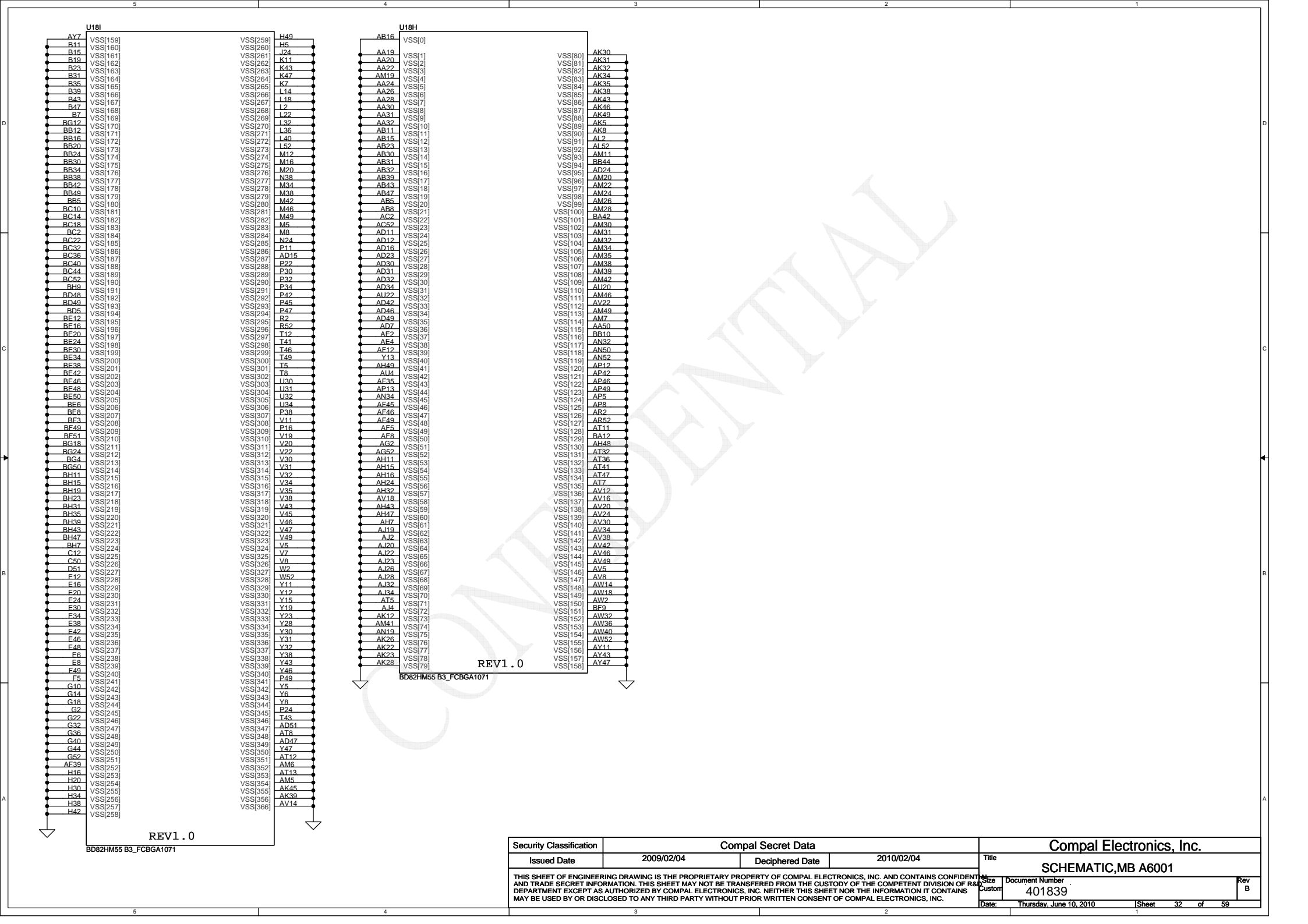
Compal Electronics, Inc.

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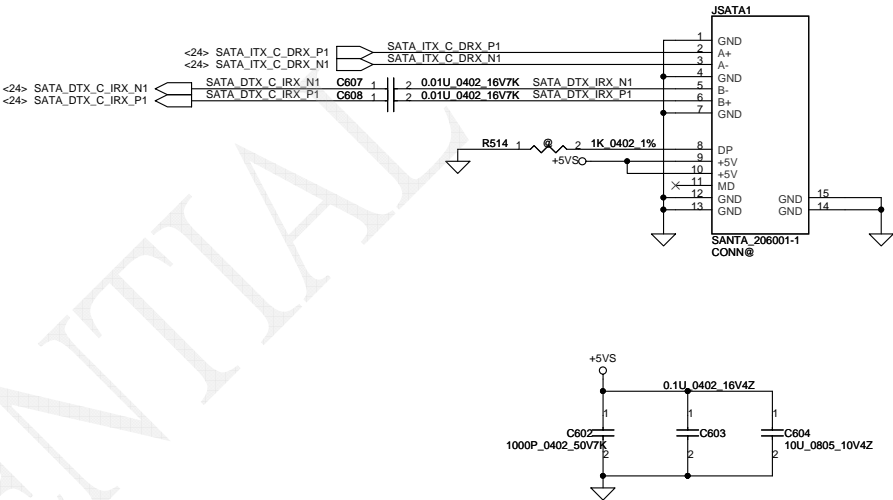
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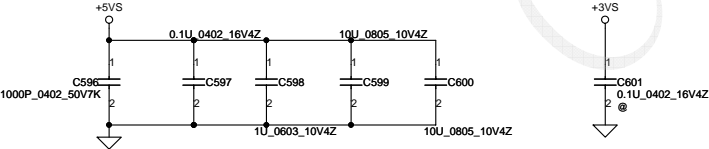
Document Number 401839
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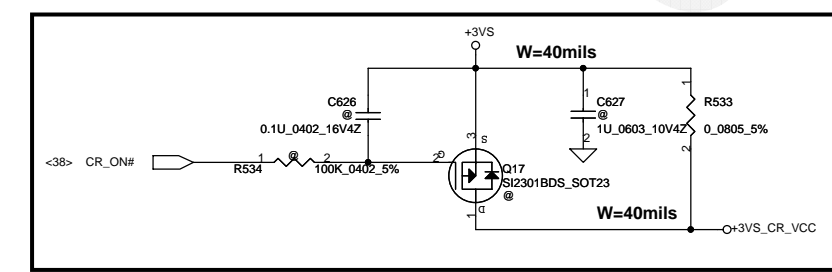
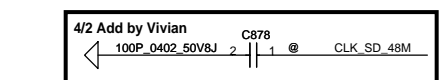
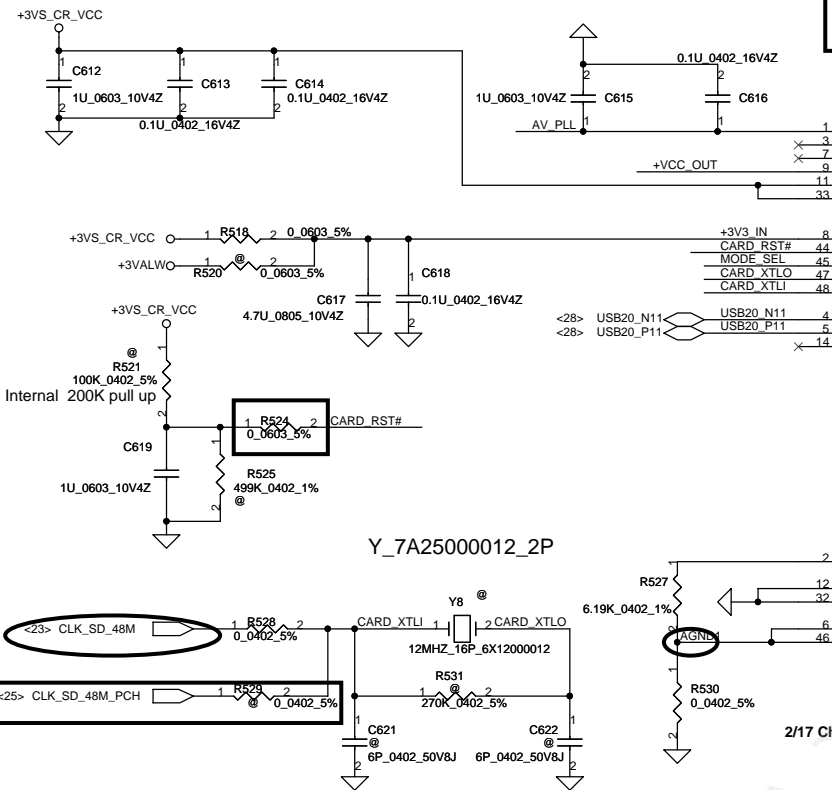
SATA ODD Conn.



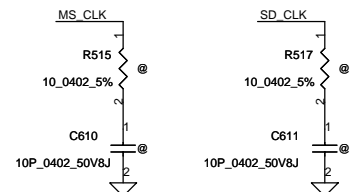
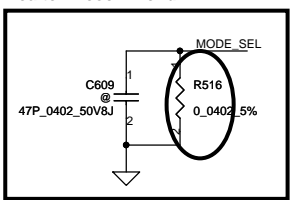
SATA HDD Conn.



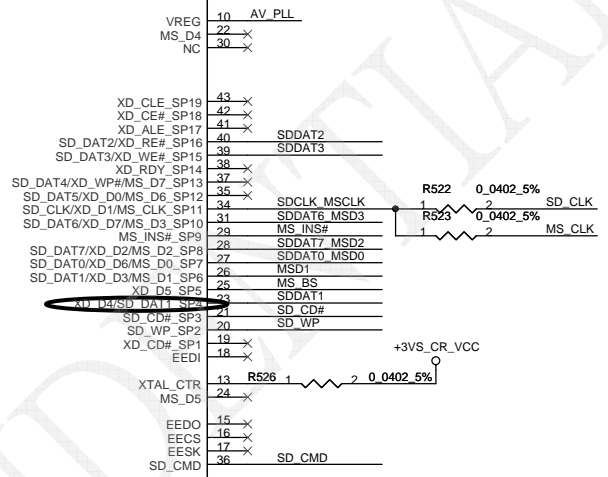
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Realtek Recommend

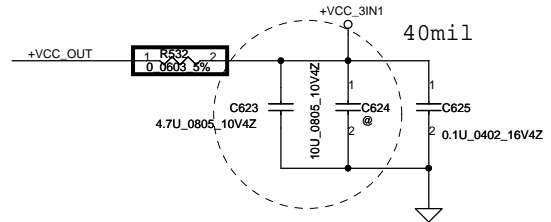


AV_PLL 20mil (+1.8V internal regulator)



SIC RTS5159-GR LQFP 48P CARD READER

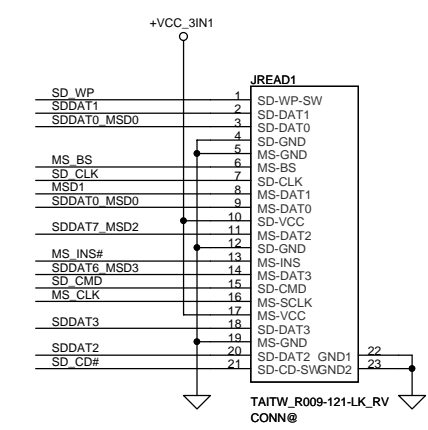
2/17 Change Part number of U25 from SA00001NK10 to SA00002YP00

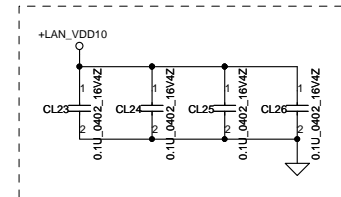
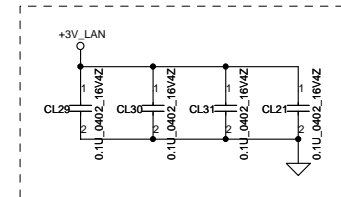
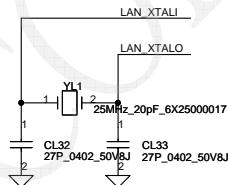
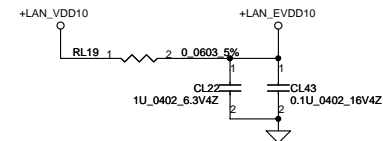
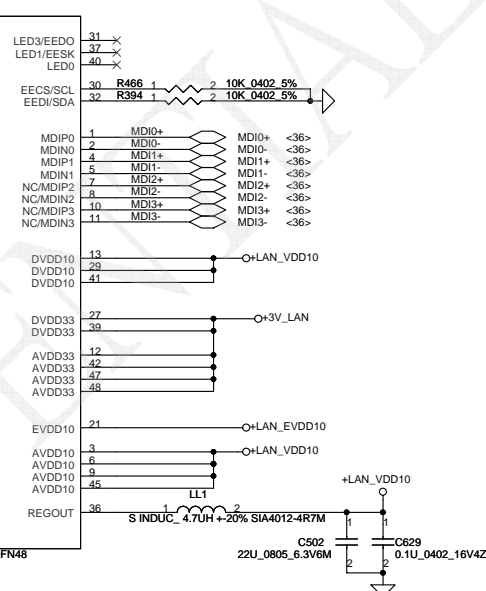
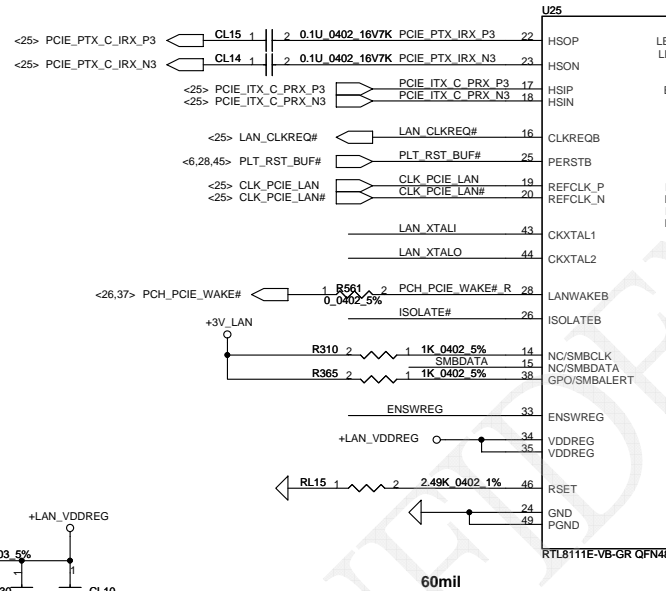
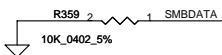
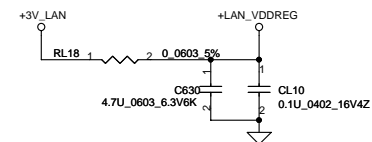
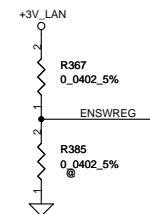
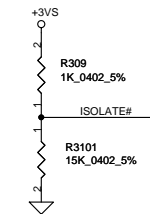
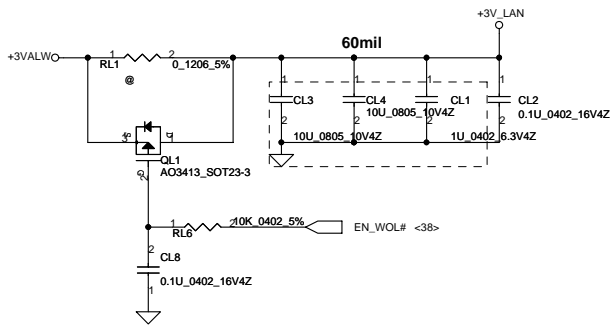


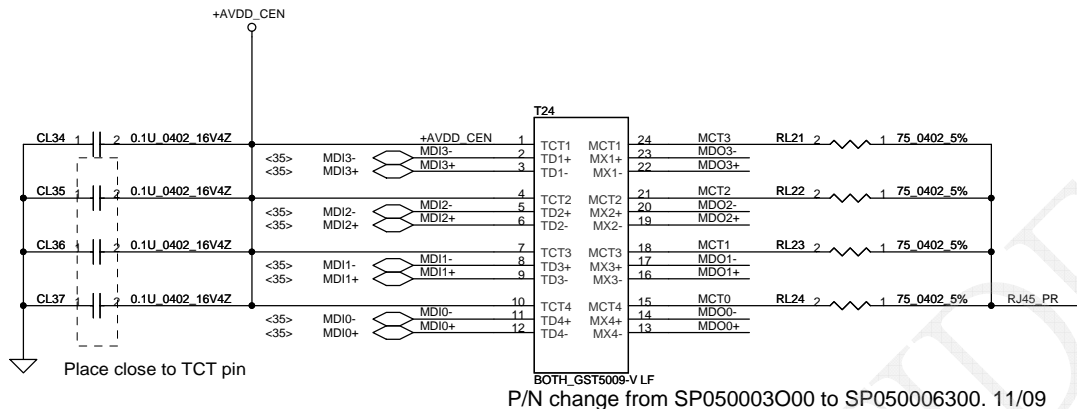
Add C822 4.7u and reserve C808 10u for cost down Michael 2008/5/30

SD,MMC,MS multi-function pin define

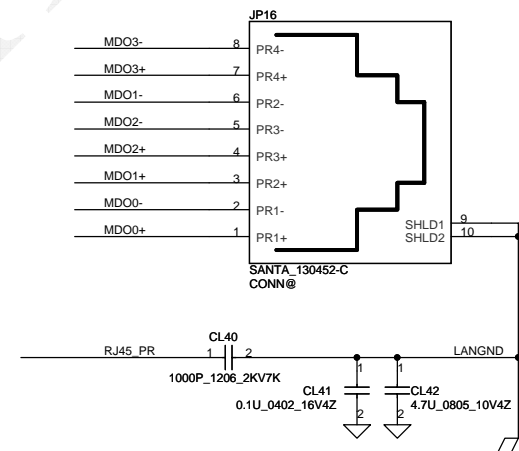
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1			
SP2	SDWP#		
SP3	SDCD#		
SP4	SDCDAT1		MSWR
SP5			MSBS
SP6			MSCDAT1
SP7	SDCDAT0		MSCDAT0
SP8	SDCDAT7		MSCDAT2
SP9			MS_INS#
SP10	SDCDAT6		MSCDAT3
SP11	SDCCLK		MSCCLK
SP12	SDCDAT5		MSCDAT6
SP13	SDCDAT4		MSCDAT7
SP14			
SP15	SDCDAT3		
SP16	SDCDAT2		
SP17			
SP18			
SP19			





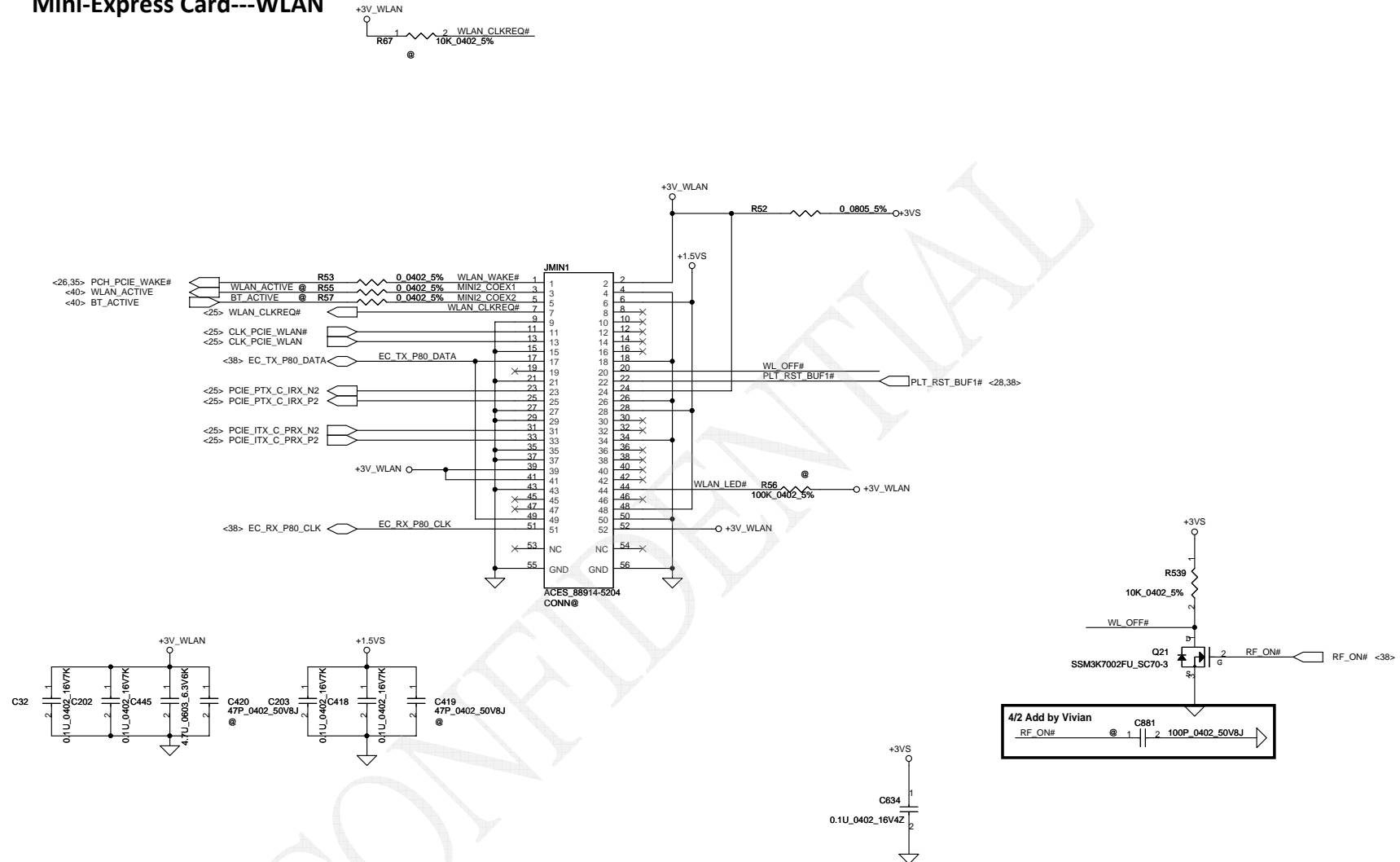


Lan Conn.

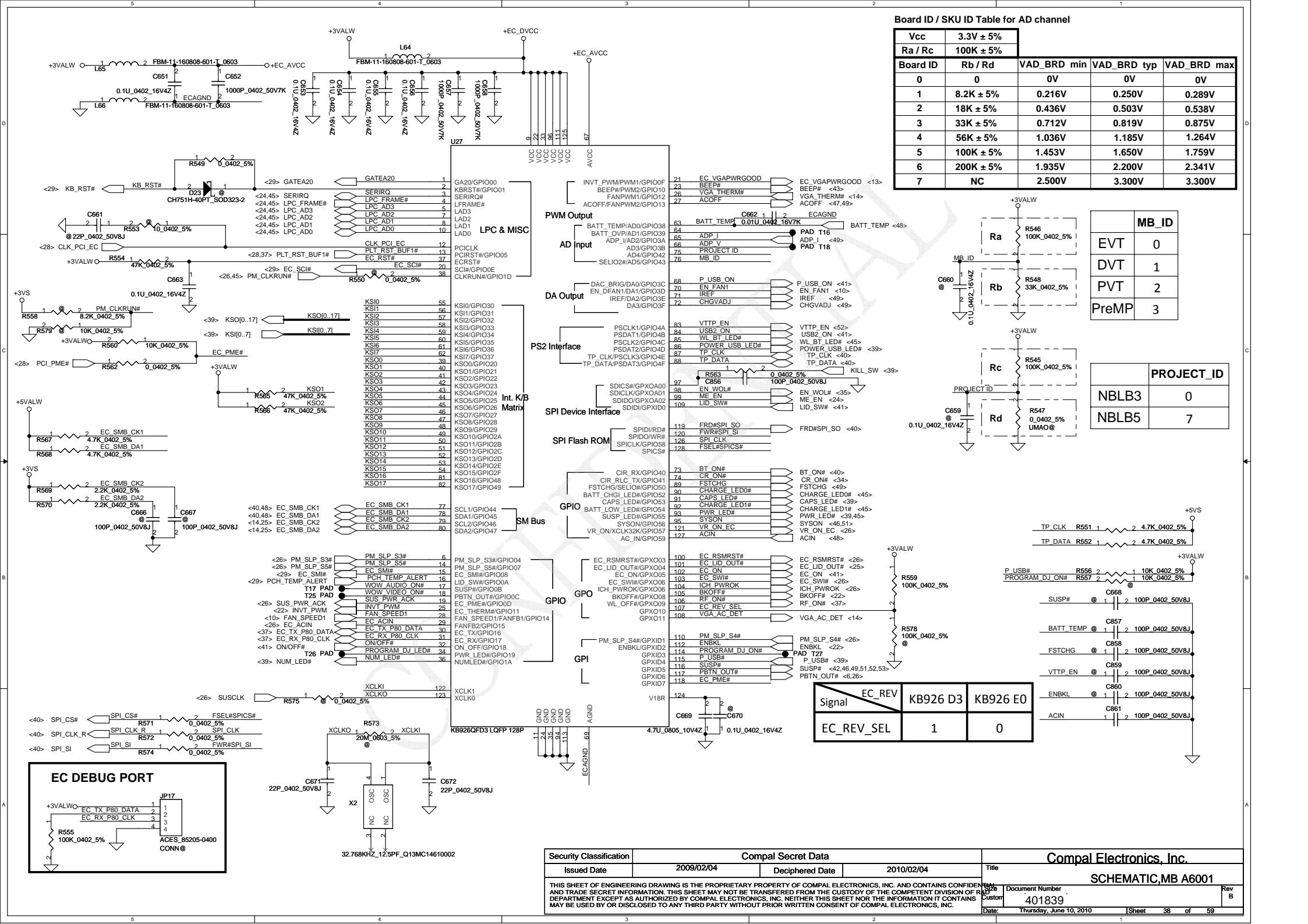


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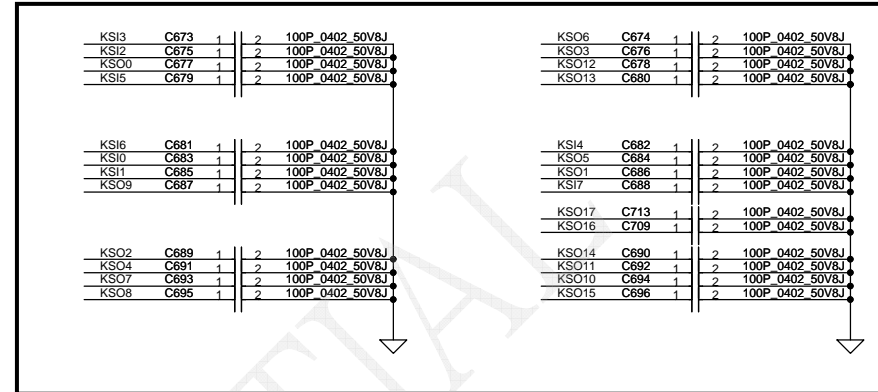
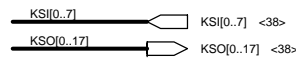
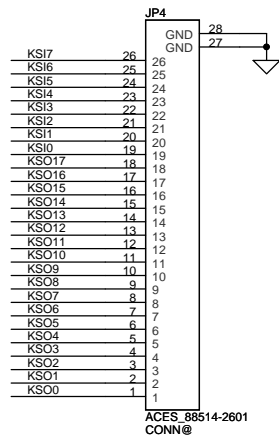
Mini-Express Card---WLAN



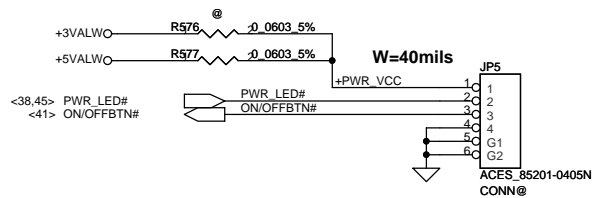
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								Customer	401839		
								Date:		Thursday, June 10, 2010	



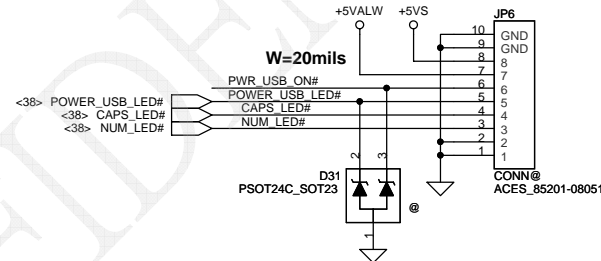
INT_KBD Conn.



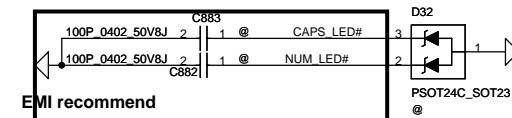
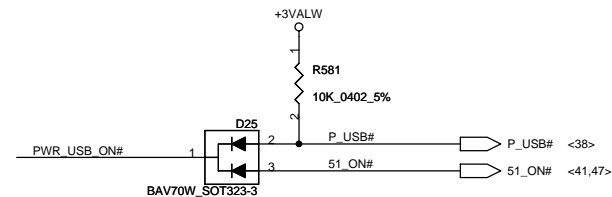
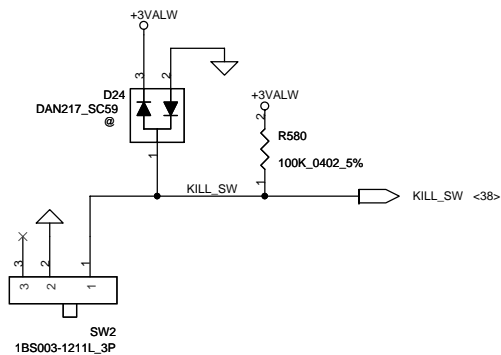
Power BTN Board Conn



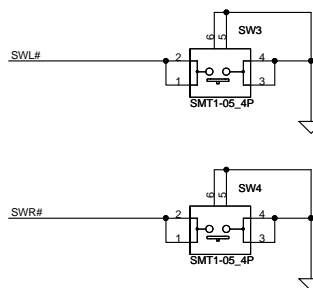
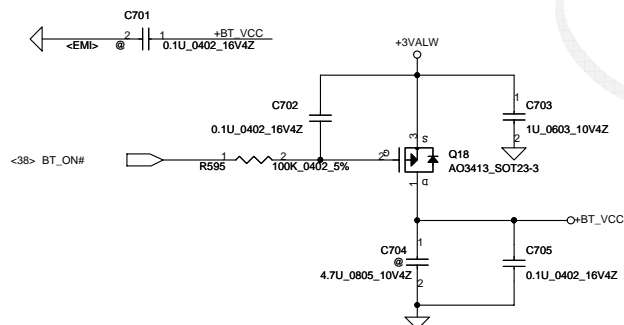
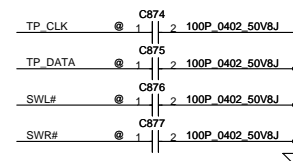
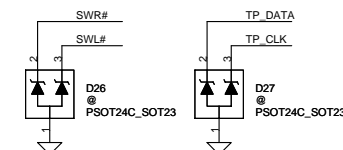
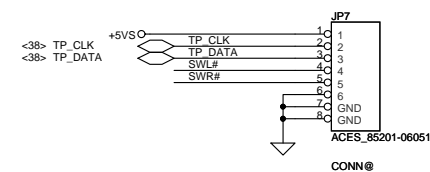
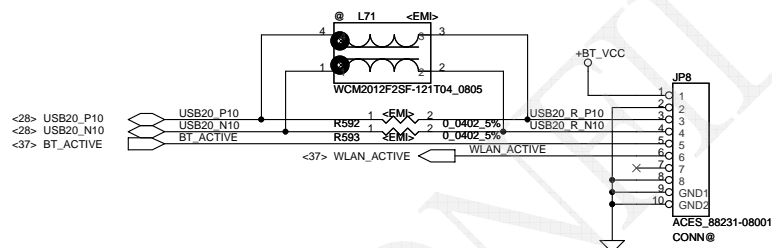
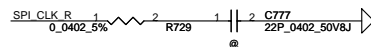
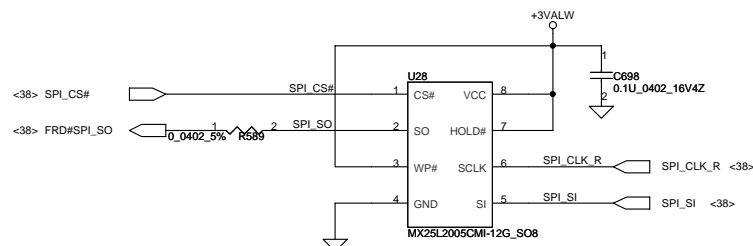
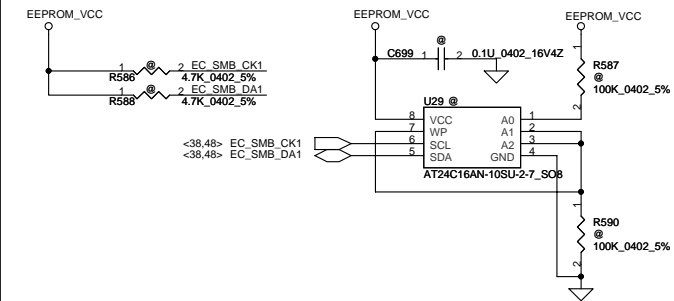
Function board conn



Kill SWITCH



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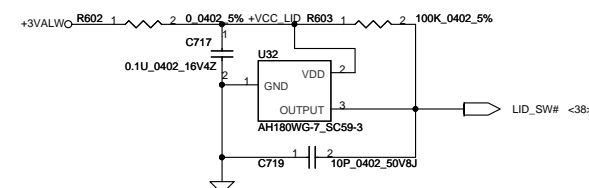
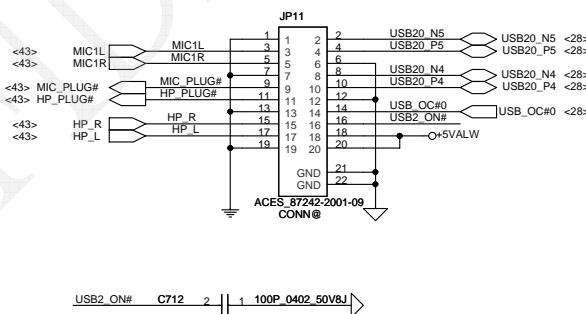
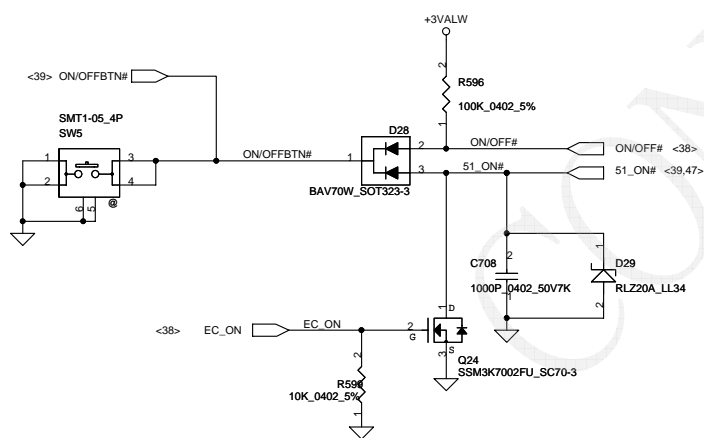
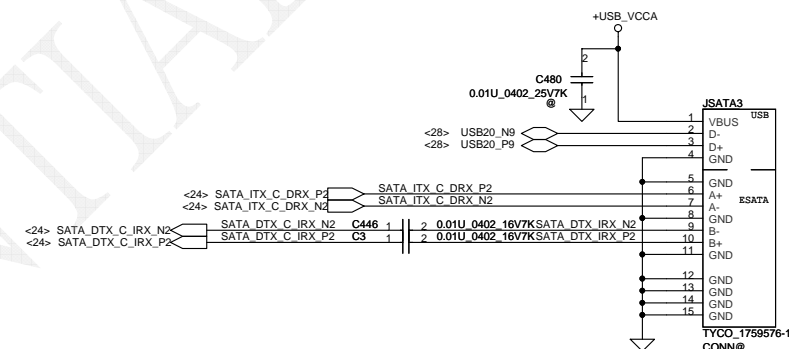
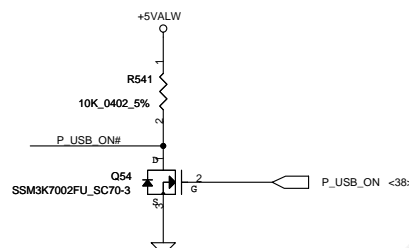
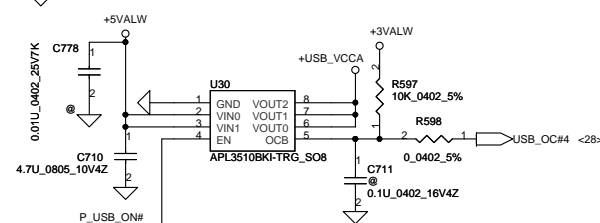
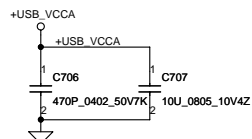


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APL3510 □□□-□□□
APL3511

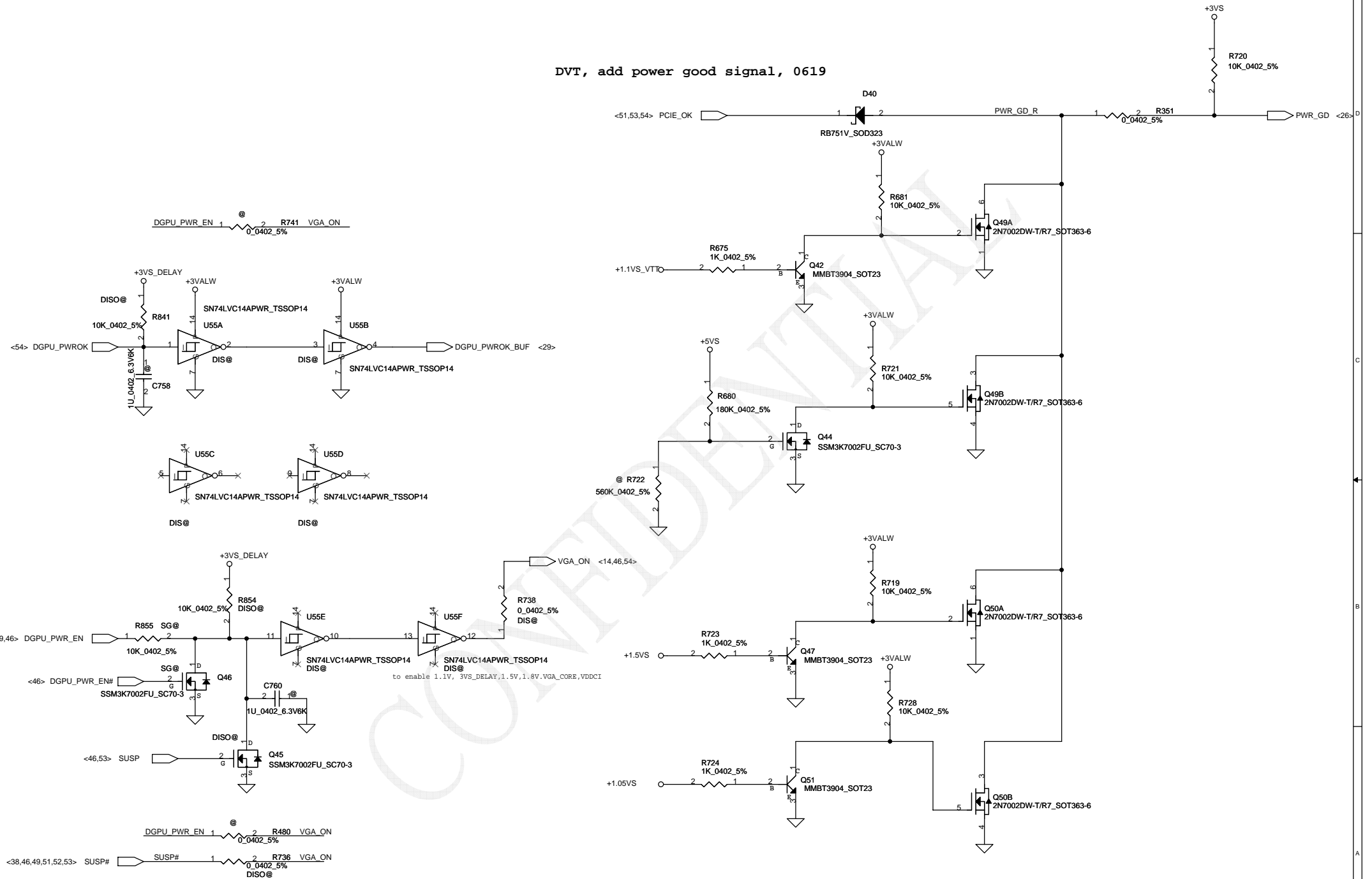
Assembly Material
Handling Code
Temperature Range
Package Code
Output Current/EN Function

Package Code
K : SOP-8 X : MSOP-8 B : SOT-23-5
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Output Current/EN Function
A : 2A/Active High B : 2A/Active Low
C : 1A/Active High D : 1A/Active Low
Assembly Material
G : Halogen and Lead Free Device

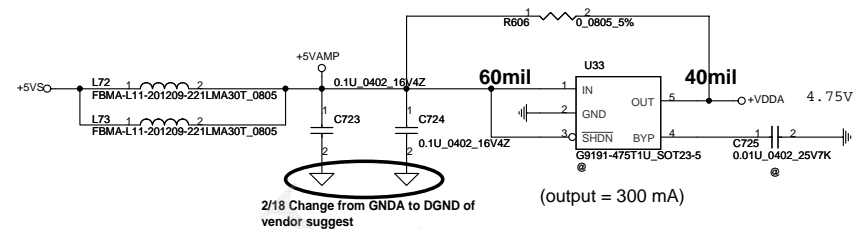
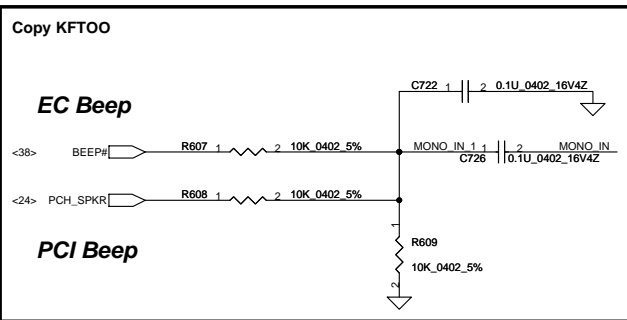


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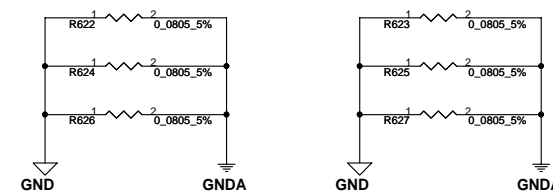
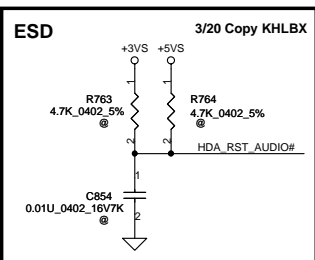
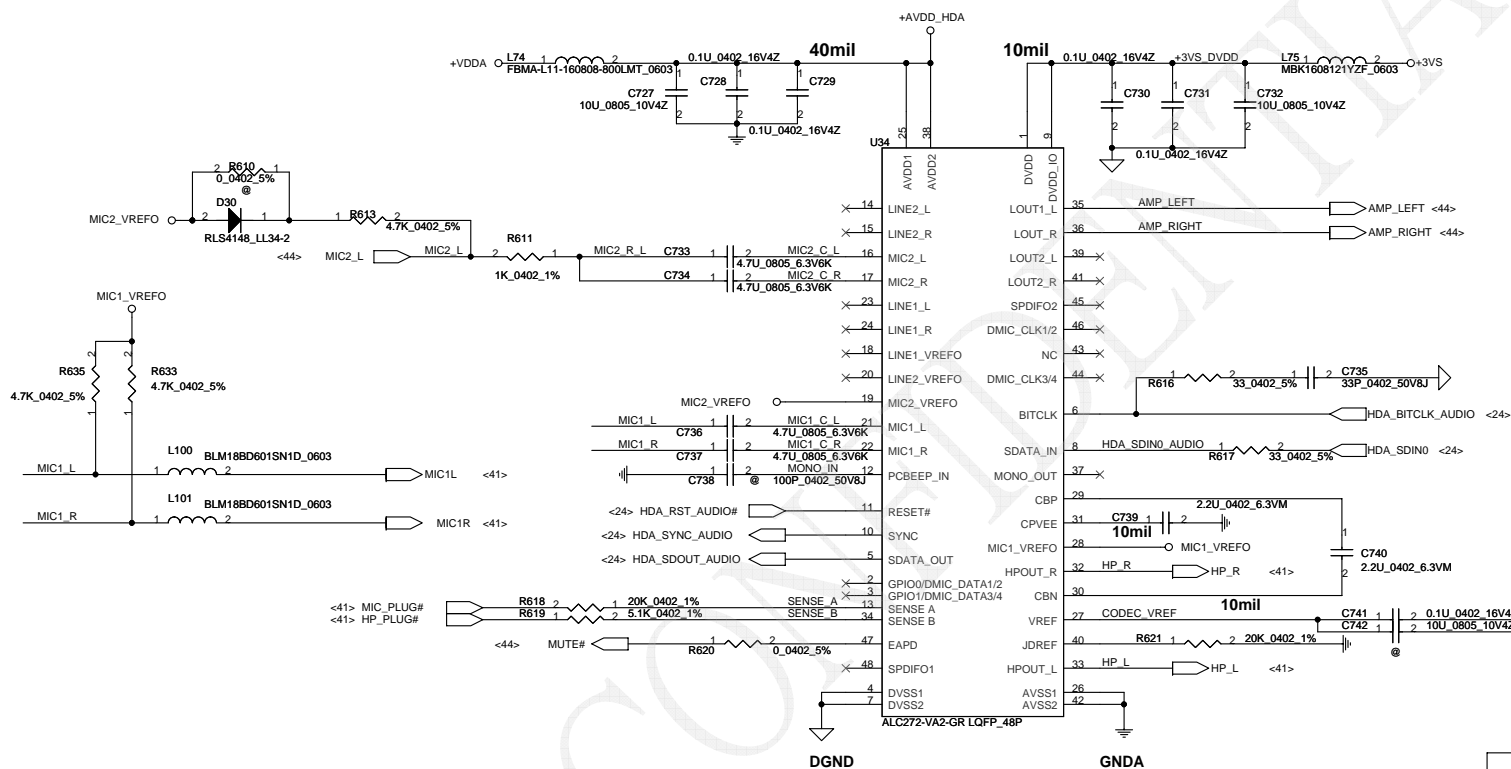
DVT, add power good signal, 0619



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HD Audio Codec

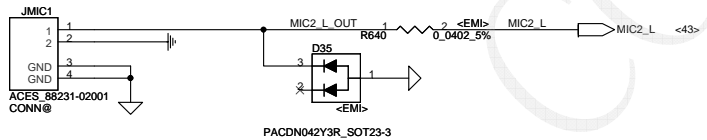
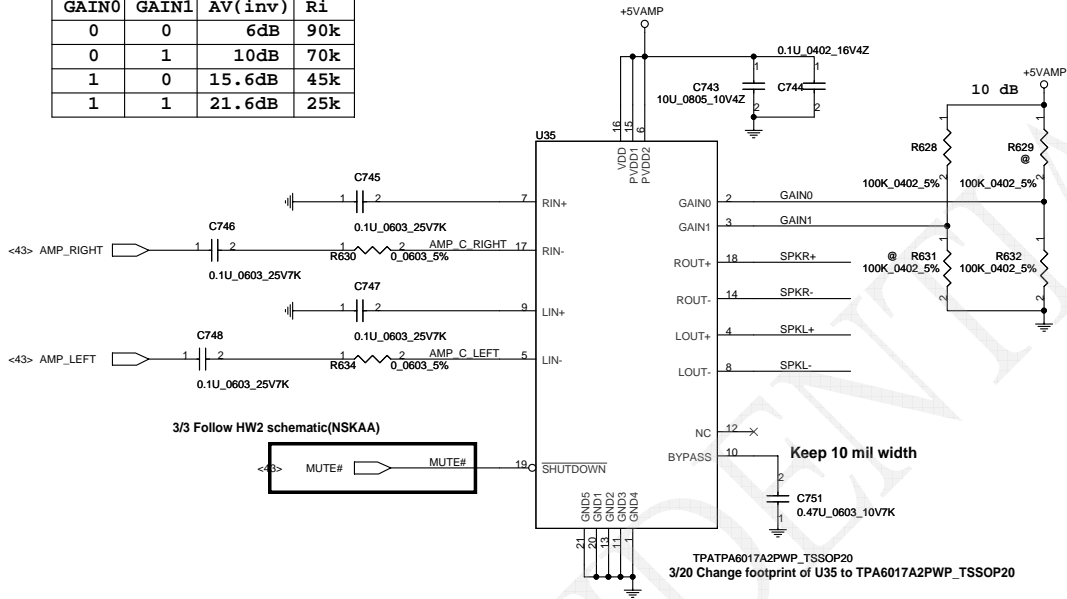


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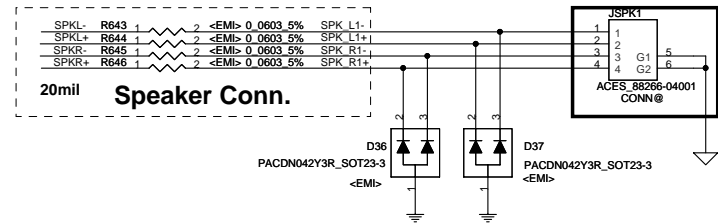
Compal Electronics, Inc.

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GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



Int. Speaker Conn.

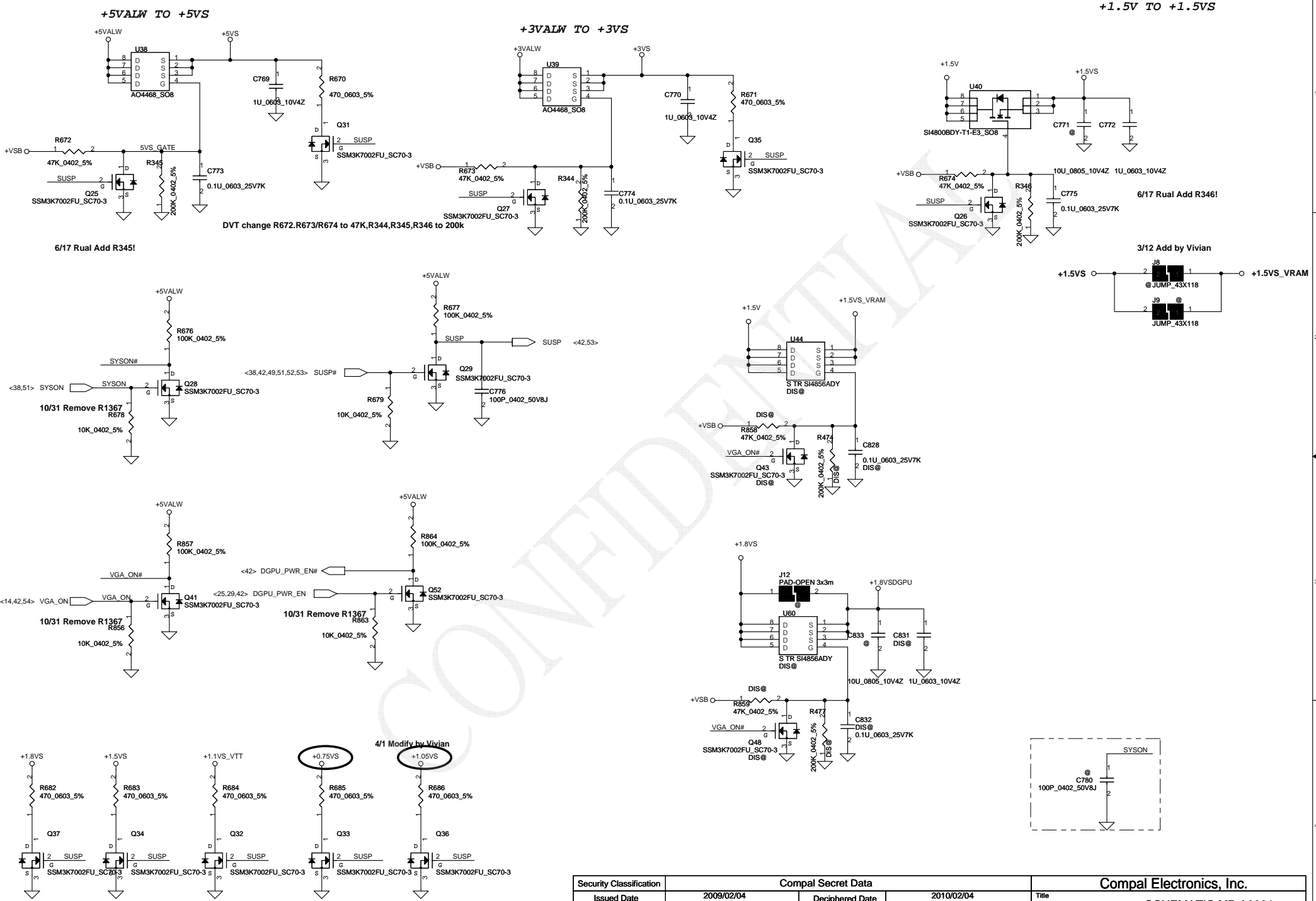


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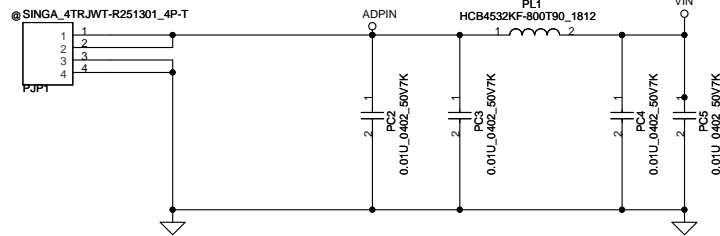
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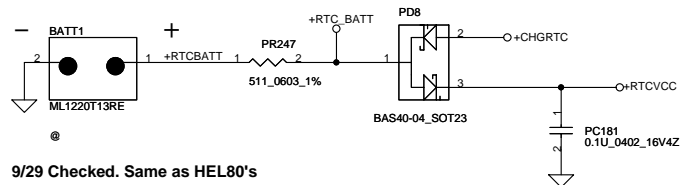
DC301008L00



RTC Battery

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

9/29 modified to follow ISKAA



Reserve another location

BOM structure comment

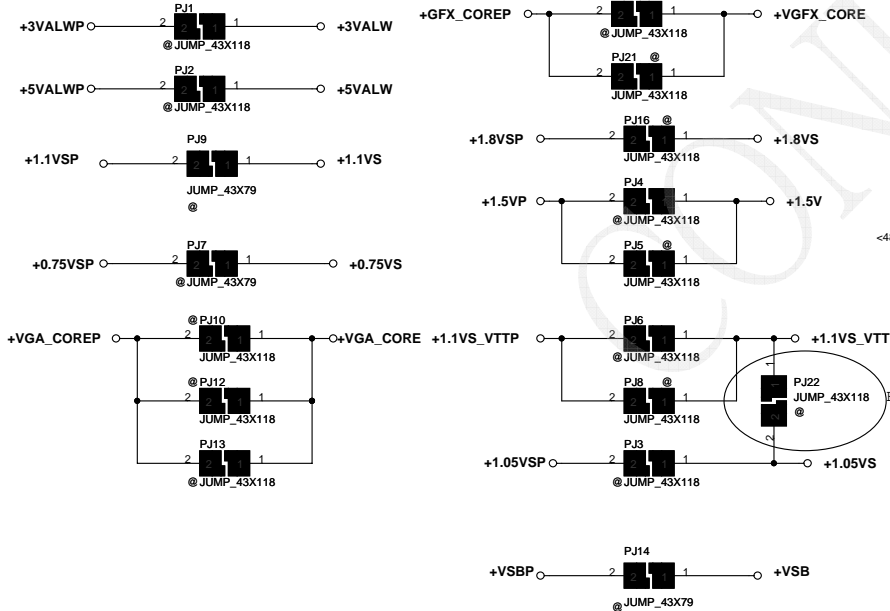
@ ==>unpop

UMA@==>UMA sku only

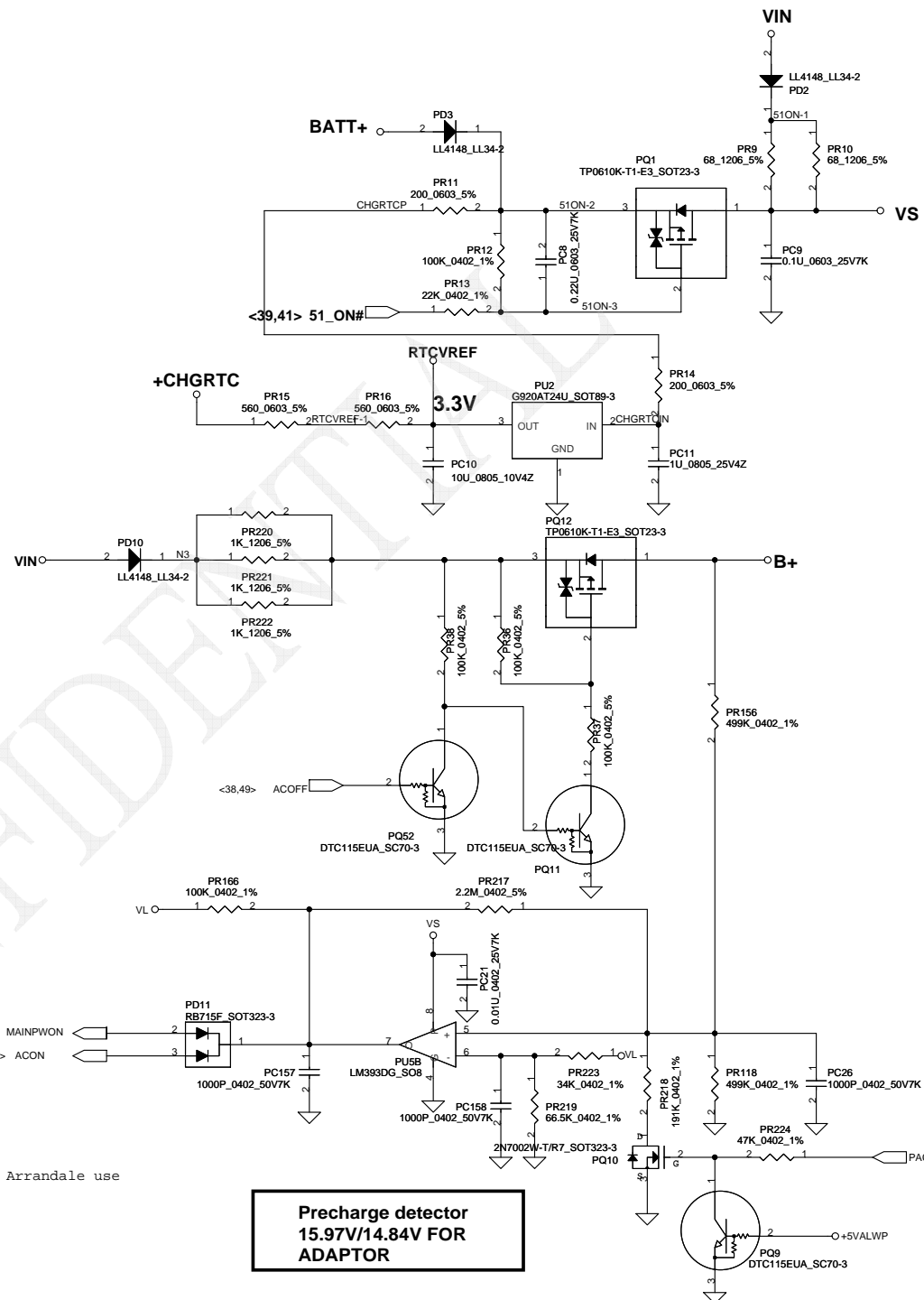
DIS@==>DIS sku only

06/24 Rual remove BATT2!

SP093MX0000

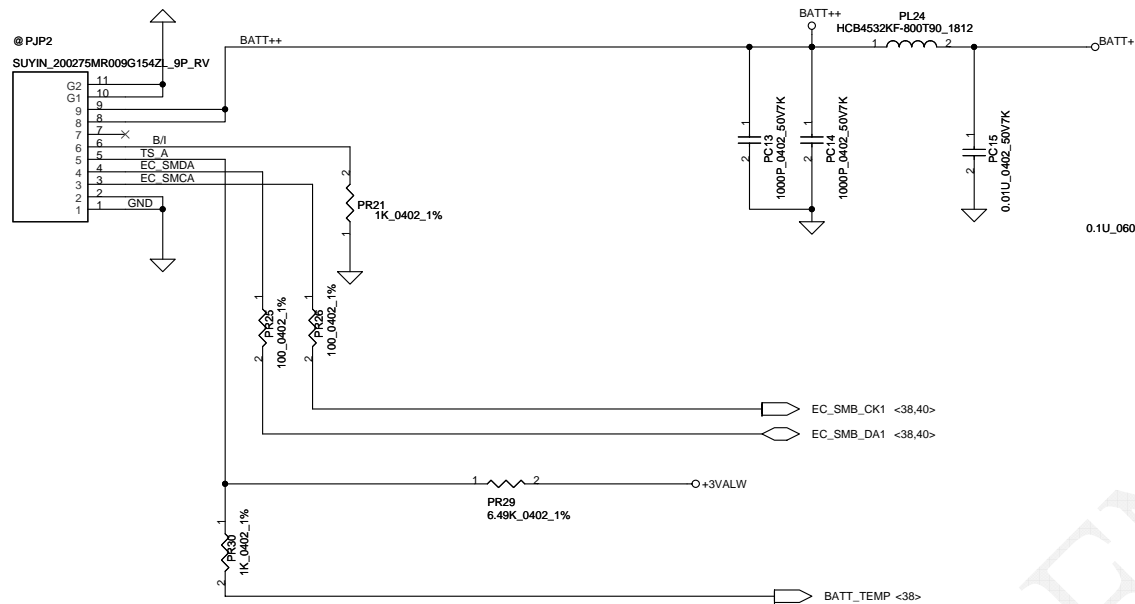


For Arrandale use

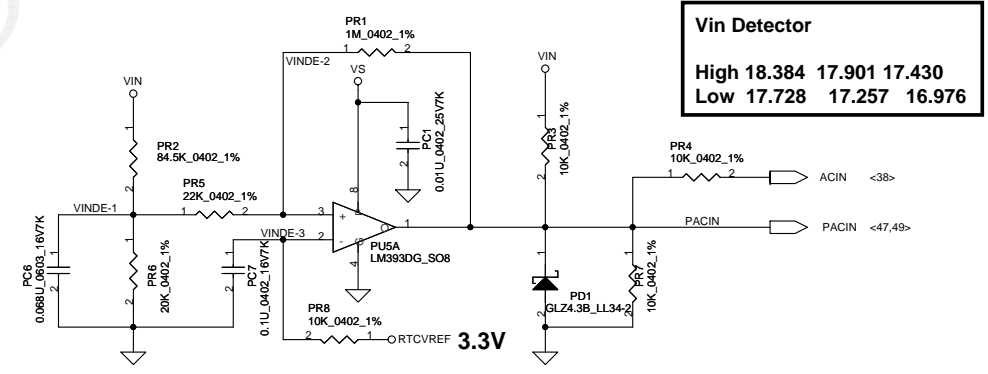
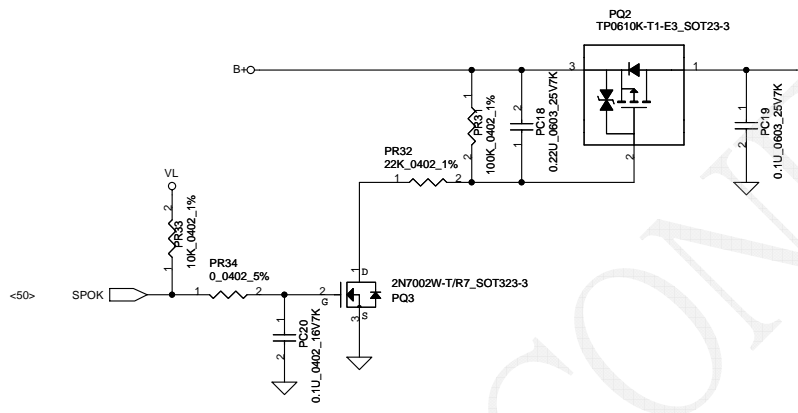
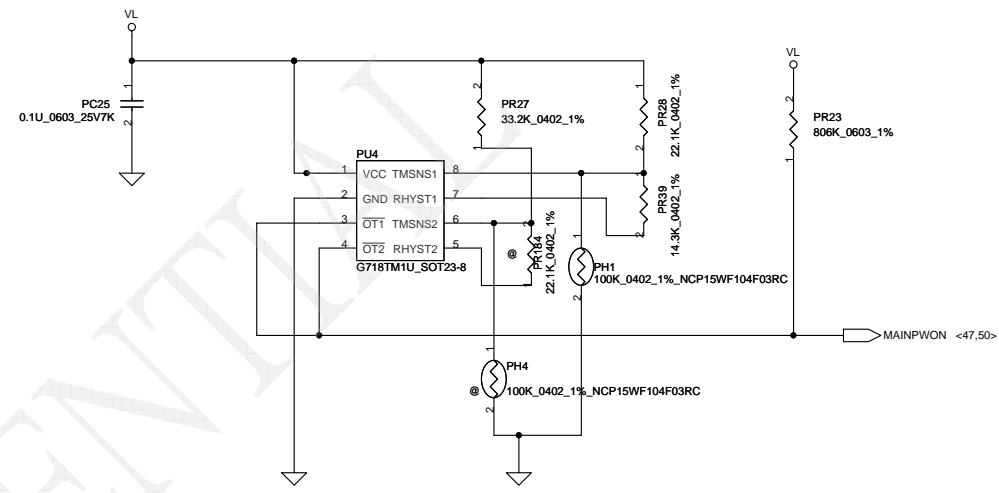


Precharge detector
15.97V/14.84V FOR
ADAPTOR

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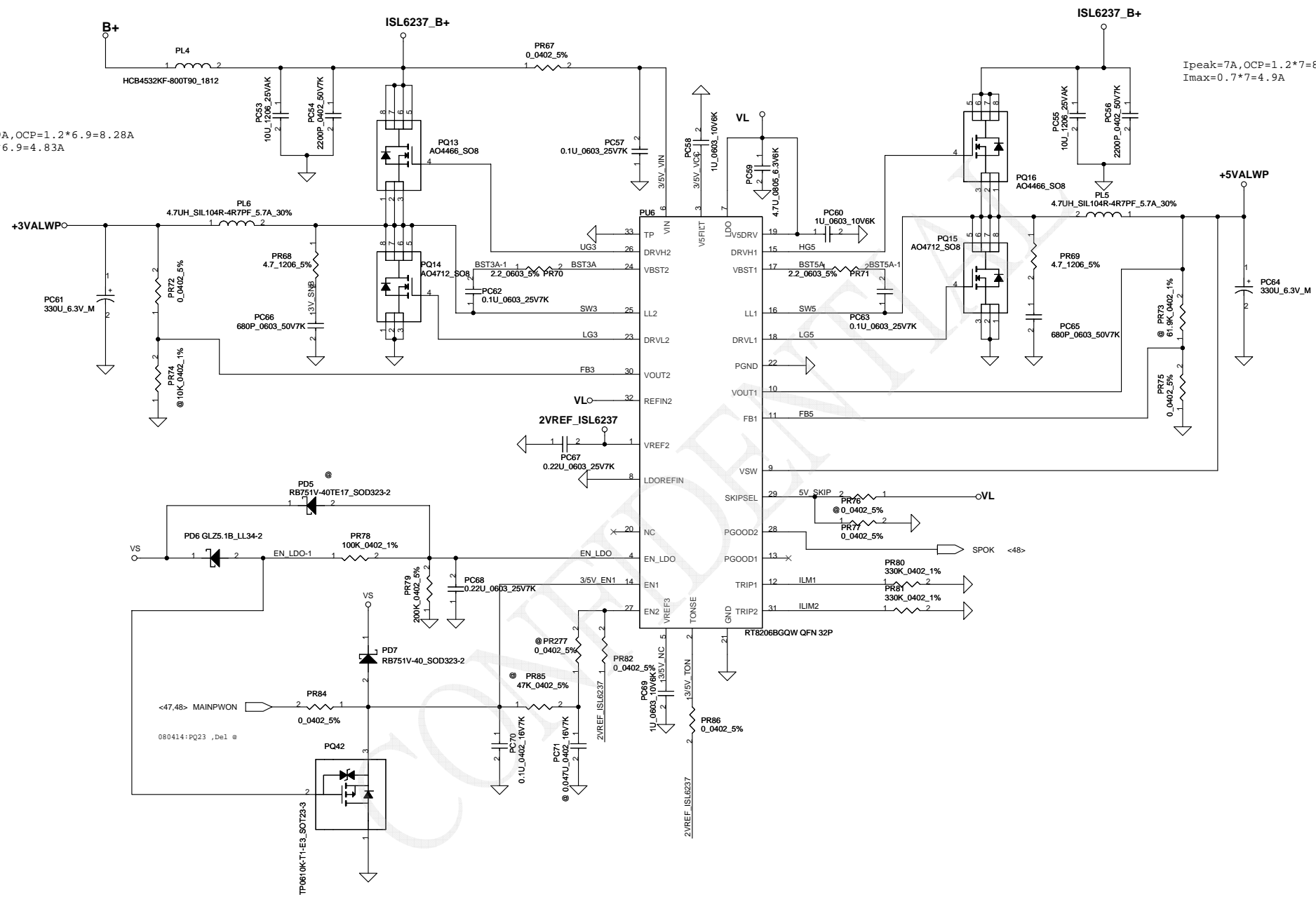
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 70 degree C



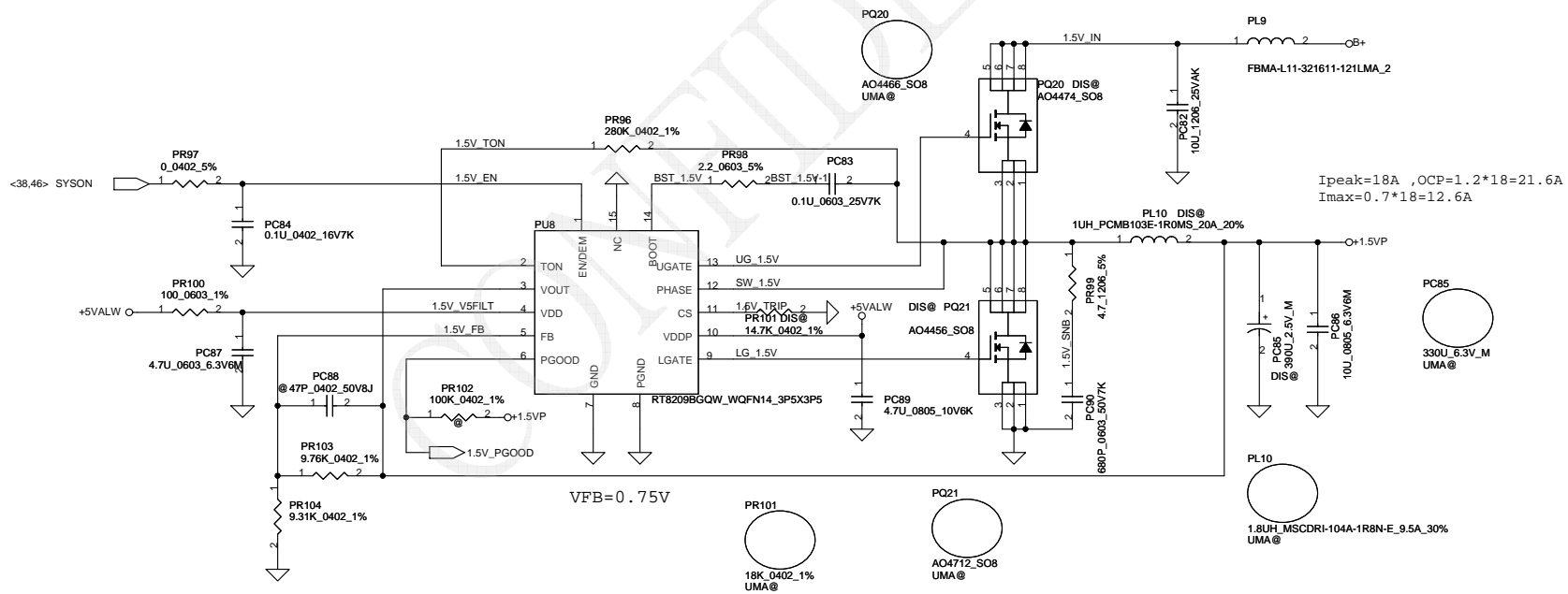
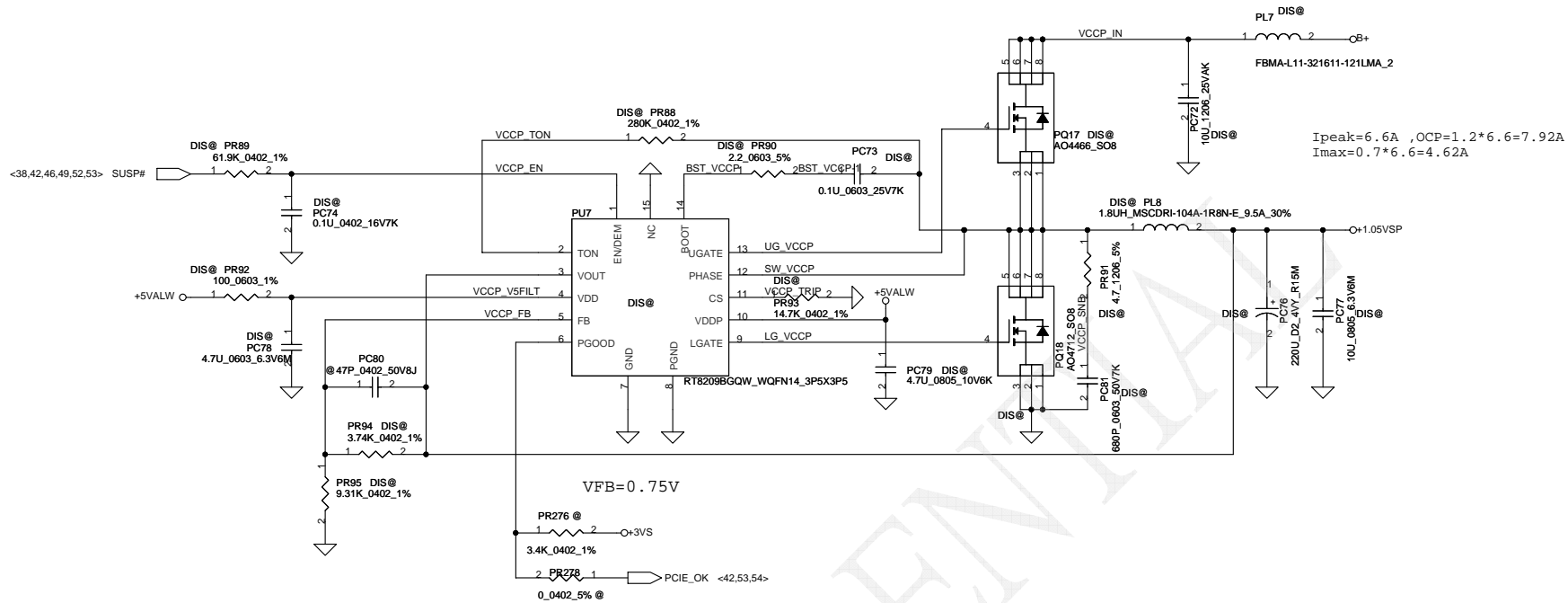
Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976

Ipeak=6.9A, OCP=1.2*6.9=8.28A
Imax=0.7*6.9=4.83A

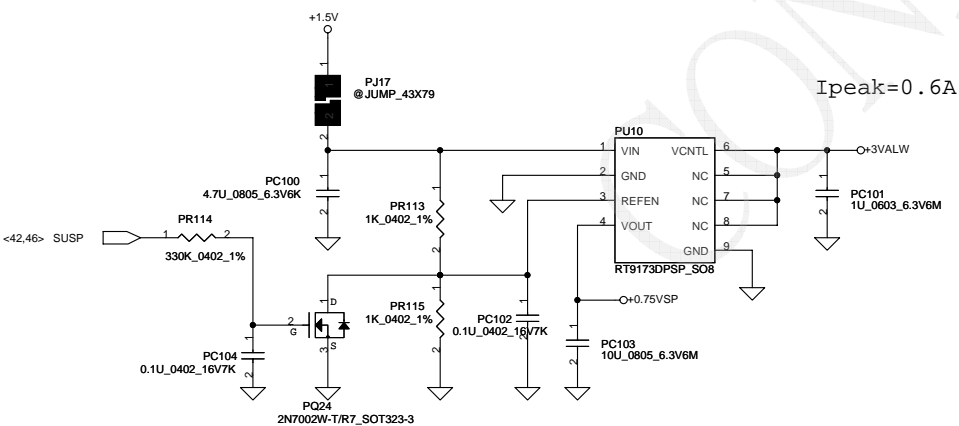
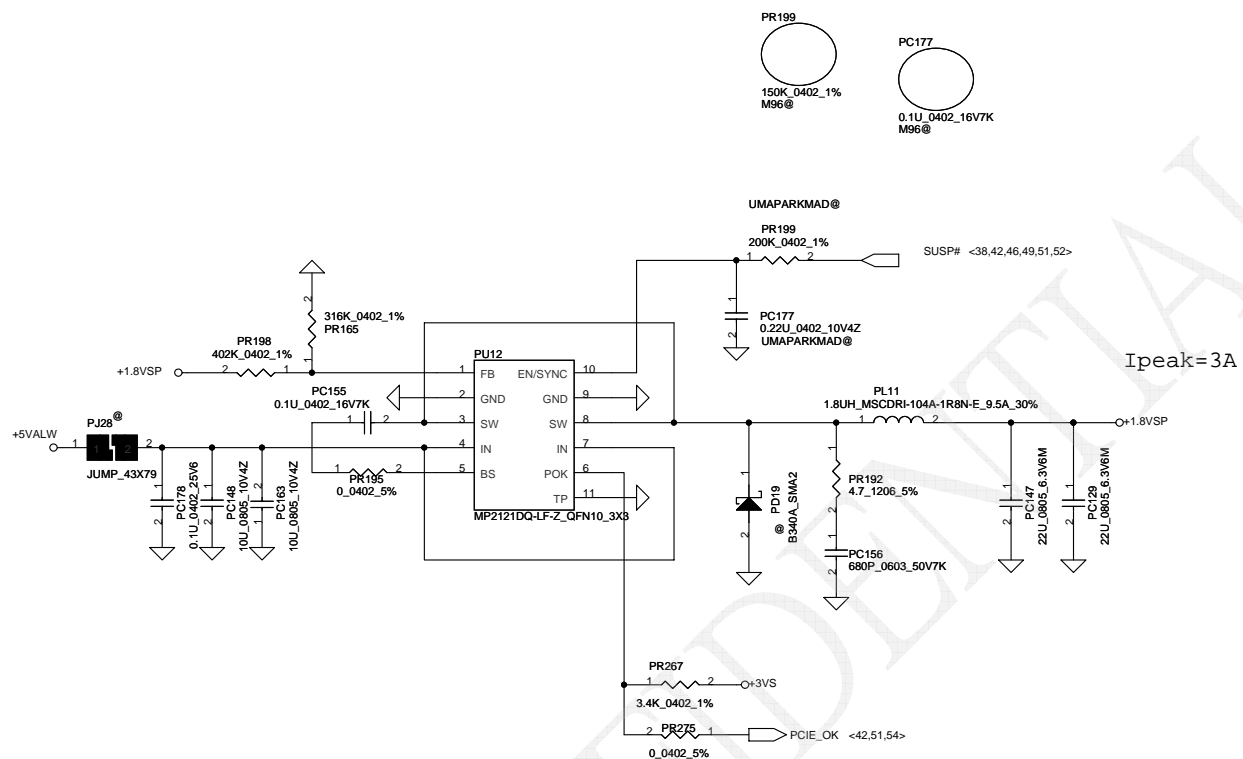
Ipeak=7A, OCP=1.2*7=8.4A
Imax=0.7*7=4.9A



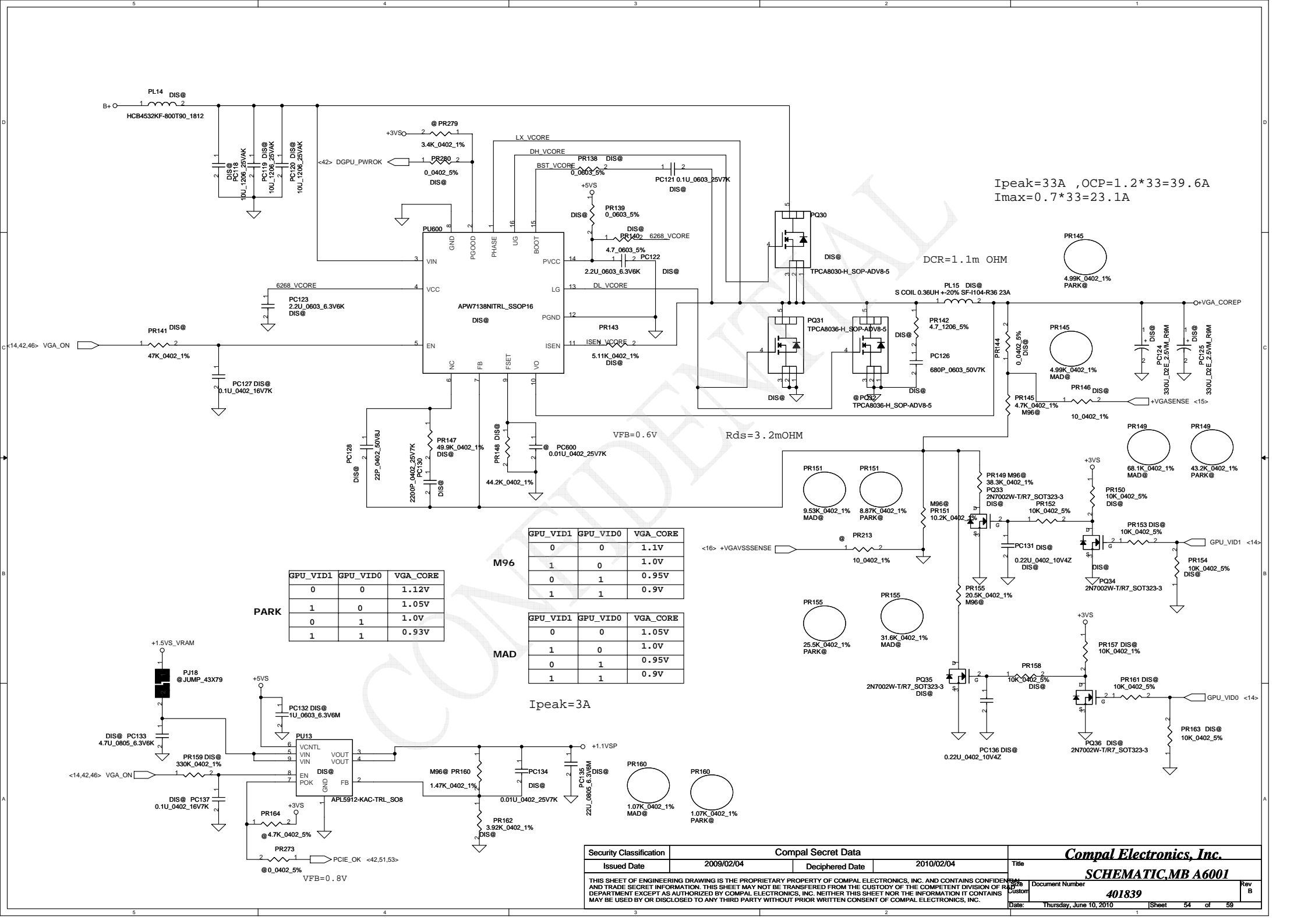
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Ipeak=33A ,OCP=1.2*33=39.6A
Imax=0.7*33=23.1A

DCR=1.1m OHM

VFB=0.6V Rds=3.2mOHM

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.1V
1	0	1.0V
0	1	0.95V
1	1	0.9V

M96

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

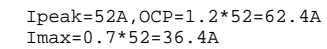
MAD

Ipeak=3A

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.12V
1	0	1.05V
0	1	1.0V
1	1	0.93V

PARK

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dy
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	can't use PWM to control brightness.	use PCH to control brightness in all SKU.	0.2	22	remove U47, R861,C825; U48; add R844, R827	01/30	DVT
2	Cost down	Cost down	0.2	23	Change Y6 from SJ100002600 to SJ114P3M730	01/30	DVT
3	Cost down	Cost down	0.2	20,21	change D7 and D15 to SCS00003H00	01/30	DVT
4	Cost down	Cost down	0.2	22	delete D18 , change R311 from 4.7K to 10K and pull down to GND.	01/30	DVT
5	Cost down	Cost down	0.2	22,40	change Q16&Q18 from SB923010020 to SB934130000 (AO3413)	01/30	DVT
6	Cost down	Cost down	0.2		delete C433, C404;C852; C851;C401;C399; C364	01/30	DVT
7	Cost down	Cost down	0.2	9,30	Change R242;R501;R502;R504 from SD00000S000 to SD002000080 (0805 0ohm)		
8	Cost down	Cost down	0.2		delete C339;C336;C334		
9	Cost down	Cost down	0.2	38	delete crystal for EC		DVT
10	Cost down	Cost down	0.2	35	change YL1 from SJ100003300 to SJ125P0M200		DVT
11	Cost down	Cost down	0.2	35	change QL1 from SB000005X80 to SB934130000 (AO3413)		DVT
12	Cost down	Cost down	0.2	41	change U30 from SA005280110 to SA000039E00		DVT
13	Cost down	Cost down	0.2	39,41	change D25&D28 from SC2N202U010 to SC600000B00		DVT
14	EMI Reserved.	EMI Reserved.	0.2	20	Add R865 and R866 on HDMI DDC signals for EMI		DVT
15	EMI&ESD Reserved.	EMI&ESD Reserved.	0.2	39	add D31, D32 and c838.		DVT
16		株y! n%?0 = ""	0.2	22		2/8	DVT
17		? ? n% ? h %-01/30					DVT
18		P? 統y! n%?0 =					
19		"" 0 !					
20							
21							
22							
23							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD PQ64 in BOM	BOM STRUCTURE ERROR	0.1	51	Delete error bom structure	11/12	EVT
2	Battery OTP set	Battery OTP set	0.1	50	Change pr27 from 10k to 33.2k (sd034332280)	11/12	EVT
3	For material EOL issue	For material EOL issue	0.1	51	change pq4,pq5,pq6 from ao4407 to ao4407a (sb00000d100)	11/12	EVT
4	PH801 part number change	PH801 part number change	0.1	58	change ph801 from sl200000581 to sl200000500	11/18	EVT
5	output voltage unstable	output voltage unstable	0.1	55	change pc129,pc147 from 4.7u to 22u(se000000i10)	11/18	EVT
6	for material shortage issue	for material shortage issue	0.1	51	change pc22,pc23,pc24 from sel42475k80 to se000006r80	11/19	EVT
7	For +3valw&5valw enable singal rising time delay	For +3valw&5valw enable singal rising time delay	0.1	52	change pr23 from 100k to 806k(sd014806380)	11/25	EVT
8	cost down	cost down	0.1	52	del pr830(sd034300080)	11/25	EVT
9	Not need	cost down	0.1	50	del pr22(sd034100180)	12/08	DVT
10	cost down	cost down	0.1	53	change pl11 from 2.2u to 1.8u(sh000008u80)	12/18	DVT
11	cost down	cost down	0.1	49	del pr225,pr226,pr265,pc175	12/24	DVT
12	cost down	cost down	0.1	56	change pq801 from si4686 to tpca8030 (sb00000hl00)	12/26	DVT
13	cost down	cost down	0.1	49	change pr35 from 1206 size to 2512 size (sd000001f00)	12/26	DVT
14	pl3 temperature is too hot when charge	pl3 temperature is too hot when charge	0.1	49	change pl3 from sh00000e300 to sh162100m10	12/26	DVT
15	cost down	cost down	0.1	51	change pq20 from ao4474 to ao4466 (sb00000cg00) UMA	12/26	DVT
16	cost down	cost down	0.1	51	change pq21 from ao4456 to ao4712 (sb00000aj00)UMA	12/26	DVT
17	cost down	cost down	0.1	51	change pl10 from 1.0u to 1.8u (sh000008u80)UMA	12/26	DVT
18	cost down	cost down	0.1	51	change pc85 from 390u to 330u (sf000001g00)UMA	12/26	DVT
19	cost down	cost down	0.1	48,49	change pq3 ,pq10,pq55,pq57,pq64 to sb000006800	01/21	DVT
20	for material shortage issue	for material shortage issue	0.1	56	change pq31 ,pq26,pq44,pq38,pq802 to sb00000hr00	01/21	DVT
21	for material shortage issue	for material shortage issue	0.1	47	change pd2 ,pd3,pd10 to sc100001y80	01/21	DVT
22	for material shortage issue	for material shortage issue	0.1	49	change pd7 ,pd18,pd20 to scs00000z00	01/21	DVT
23	for material shortage issue	for material shortage issue	0.1	48	change pd1 to sc400001200	01/21	DVT

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1	for material shortage issue	for material shortage issue	0.1	50	change pd6 to sc400001300	01/21	DVT
2	for material shortage issue	for material shortage issue	0.1	49	change pd11,PD15 to scsh715f080	01/21	DVT
3	for material shortage issue	for material shortage issue	0.1	51	change pl17,pl19,pl15,pl802 to sh000005680	01/21	DVT
4	cost down	cost down	0.1	56	change pl16 to sm010020720	01/21	DVT
5	Change 1.1vsp power level from 1.0v to 1.1v	vga chip change from madison to M96	0.1	54	change pr160 from 1.07k to 1.47k(sd000009480)	1/29	DVT
6	ME interface	ME interface	0.1	49	change pr35 from 2512 size to 1206 size	1/29	DVT
7	OCP SETTING	OCP SETTING	0.1	52	change pr125 from 3.74k to 5.11k in UMA sku, change pr125 from 3.74k to 4.02k in DIS sku	2/2	DVT
8	OCP SETTING	OCP SETTING	0.1	51	change pr101 from 12.7k to 18k in UMA sku, change pr125 from 12.7k to 14.7k in DIS sku	2/2	DVT
9	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	0.1	55	change pq38,pq44from TPCA8036 to TPCA8028 in DIS sku	2/4	DVT
10	For madison voltage level change	For madison voltage level change	0.1	54	change pr151 from 10.2k to 9.53k(sd034953180)	2/5	DVT
11	For madison voltage level change	For madison voltage level change	0.1	54	change pr155 from 20.5k to 31.6k(sd034316280)	2/5	DVT
12	For madison voltage level change	For madison voltage level change	0.1	54	change pr149 from 38.3k to 68.1k(sd034681280)	2/5	DVT
13	For madison voltage level change	For madison voltage level change	0.1	54	change pr145 from 4.7k to 4.99k(sd034499180)	2/5	DVT
14	HW sequency request	HW sequency request	0.1	53	change pr199 from 200k to 150k for M96 VGA chip(sd034150380)	2/23	DVT
15	HW sequency request	HW sequency request	0.1	53	change pcl77 from 0.22u to 0.1u for M96 VGA chip(se076104k80)	2/23	DVT
16	H_vttpwrgd glitch issue	H_vttpwrgd glitch issue	0.1	52	change PU500 pin14 pull high voltage from +5vs to +5valw	3/22	PVT
17	fix ki for all 030 project	fix ki for all 030 project	0.1	49	change pr269 from 80.6k to 150k(sd034150380) change pr260 from 100k to 140k(sd034140380)	3/29	PVT
18	fix kv for all 030 project	fix kv for all 030 project	0.1	49	change pr274 from 15.4k to 18.2k(sd034182280)	3/29	PVT
19	for IMON setting	for IMON setting	0.1	55	change pr55 from 4.53k to 5.36k, pcl74 from 0.1u to 0.068u in UMA SKU	04/1	PVT
20	for RPM frequency setting	for RPM frequency setting	0.1	55	change pr174 from 47.5k to 69.8k,	04/1	PVT
21			0.1	47		01/21	DVT
22			0.1			01/21	DVT
23			0.1			01/21	DVT

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